

# **EA900 3-3 10-120KVA UPS**

## **Maintenance Manual**

## CONTENTS

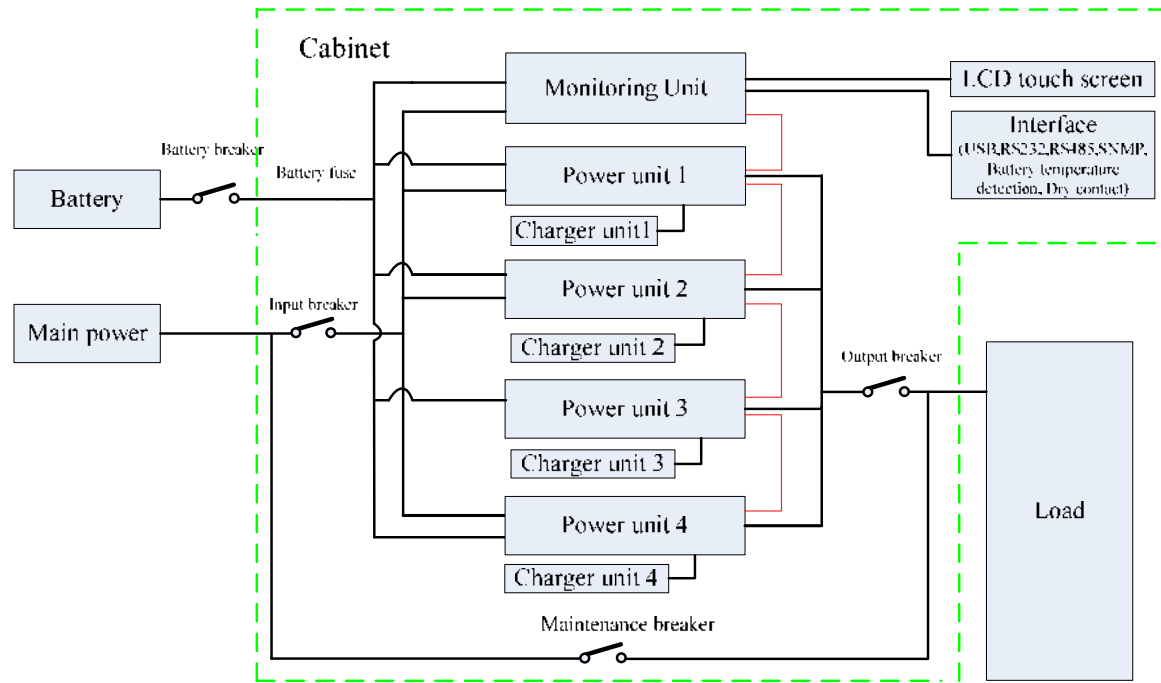
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1. Principle Block Diagram.....	4
1.1 Overall principle block diagram.....	4
1.2 Principle block diagram and topological graph of power module .....	4
1.3 Principle block diagram and topological graph of charger module.....	5
2. Principle of Power Module .....	6
2.1 Fan driving module .....	6
2.2 IGBT driving module (IGBTDR) .....	7
2.3 SCR driving module (SCRDRV) .....	9
2.4 Auxiliary power supply module (SPS).....	10
2.5 Soft start module (SOFTSTART).....	12
2.6 Input board (IP-BOARD).....	14
2.7 Rectifier module (RECTIFIER).....	16
2.8 Bypass SCR module (BPS-SCR) .....	17
2.9 Power factor correction module (PFC) .....	18
2.10 Inverter module (INVERTER) .....	21
2.11 Inductance capability board (LC-BOARD).....	22
2.12 IGBT connecting plate (IGBT-CONNECTOR) .....	25
2.13 Output board (OP-BOARD) .....	27
2.14 Output filter board (OP_EMI).....	29
2.15 Power socket connecting plate (IN_CON_Z) .....	30
2.16 Power socket connecting plate (IN_CON_T) .....	31
2.17 Lamp Panel (POWER_MODULE LED) .....	32
2.18 Control connecting plate (CNTL-CONNECTOR).....	32
2.19 Control panel (CNTL).....	35
3. Principle of Charger module .....	39
3.1 The introduction of charger module.....	39
3.2 Auxiliary power supply module (SPS).....	40
3.3 CHGR_CNTL .....	42
3.4 CHGR_PSDR.....	45
4. Principle of Monitoring Module .....	46
4.1 Communicational power supply board (COM_SPS) .....	46
4.2 Input connecting plate (INPUT_CNT).....	48
4.3 Control panel of monitoring module (MONITOR BOARD).....	49
<b>Chapter II Start Debugging of Module.....</b>	<b>50</b>
1. Start Debugging of Power Module.....	50
1.1 Power on of DC source and BUS voltage sampling .....	50
2. Start Debugging of Charger module .....	51
2.1 Main power current-limiting start and BUS voltage sampling .....	51
2.2 Measurement of charging voltage .....	52
<b>Chapter III Fault and Warning Code of Module .....</b>	<b>52</b>
1. Fault and Warning Code of Power Module.....	52
1.1 Warning code of power module .....	52

1.2 Fault code of power module.....	54
2. Fault and Warning Code of Charger module.....	55
2.1 Warning code of charger module .....	55
2.2 Fault code of charger module.....	55
<b>Appendix: .....</b>	<b>57</b>
1. Connection Diagram of Single Board of Power Module .....	57
2. Connection Diagram of Single Board of Monitoring Module .....	58

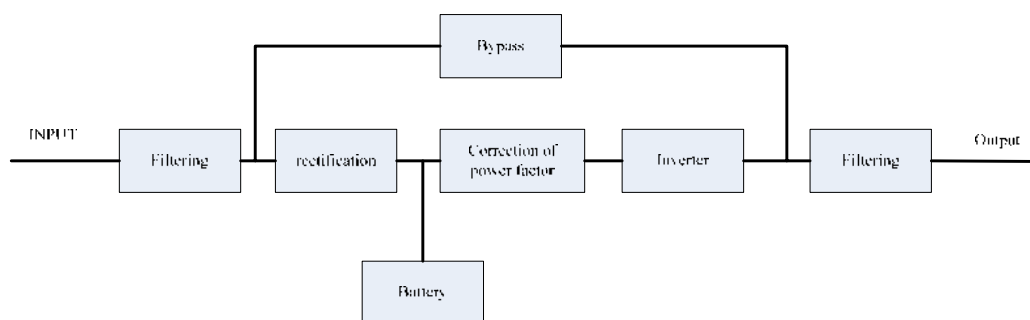
## 1. Principle Block Diagram

### 1.1 Overall principle block diagram

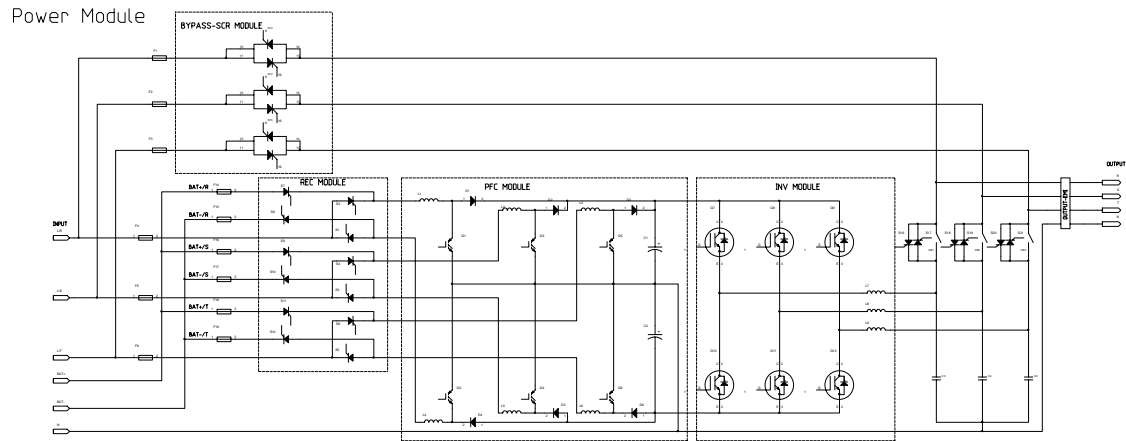


Schematic Diagram of EA900 10-120K Overall Unit Product

### 1.2 Principle block diagram and topological graph of power module

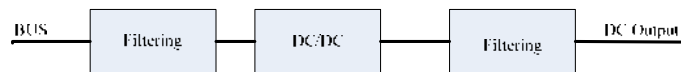


Principle Block Diagram

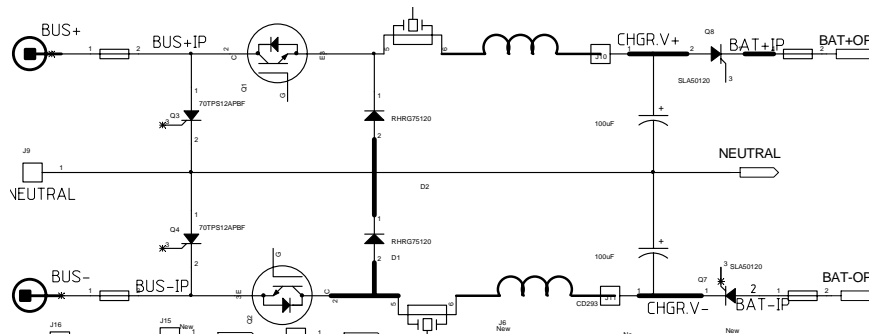


Topological Graph

### 1.3 Principle block diagram and topological graph of charger module



Principle Block Diagram



Topological Graph

- (1) Input filtering: finishing filtering of input main power to provide clean power supply for the module.
- (2) Rectification: take AC/DC switching of main power after filtering.
- (3) Correction of power factor: boost to the DC after rectification for inverter use.
- (4) Inverter: switch the AC power after boosting into stable AC output.
- (5) Bypass: it will switch to bypass mode automatically to prevent power failure of the load when UPS is overloaded or the inverter is abnormal.
- (6) DC/DC (BUCK): reduce the BUS voltage into charge voltage of the battery.
- (7) Output filtering: finishing filtering of output for the module to provide clean power supply for the load.

## 2. Principle of Power Module

Power module is composed by several functional modules, including fan driving module, IGBT driving module, SCR driving module, auxiliary power supply module, soft start module, input board, rectifier module, bypass SCR module, power factor correction/boost module, inverter module, inductance capacitor plate, IGBT connecting plate, output board, output filter board, power socket connecting plate IN\_CON\_Z, power socket connecting plate IN\_CON\_T, lamp panel, control connecting plate and control panel.

### 2.1 Fan driving module

#### 2.1.1 Introduction for functions of fan driving module

Fan of machine can accelerate heat dissipation of elements for the whole unit, and the fan driving module can achieve driving, speed adjustment and inspection of working condition of the fan. It will result in excessive temperature of elements for the machine and even explosion of the machine if the fan cannot work normally due to fault of fan driving module. In the fan driving module, FANSPD is the control signal to adjust rotate speed of the fan, magnitude of FANSPD DUTY controls rotate speed of the fan, that is, the larger DUTY is, the faster rotate speed of fan is; and FANDET is used to inspect rotate speed of the fan.

#### 2.1.2 Schematic circuit and physical map of fan driving module

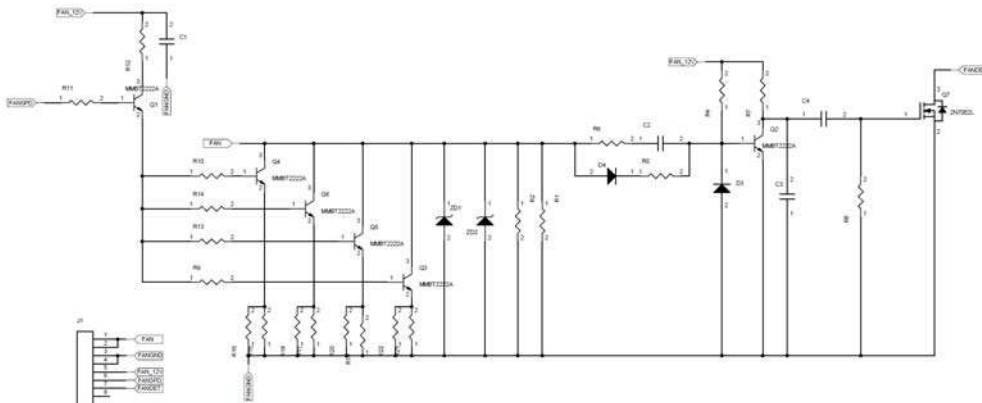


Figure 2.1.1 Schematic Circuit of Fan Driving Module



Figure 2.1.2 Physical Map of Fan Driving Module

### 2.1.3 Explanation for signal interface of fan driving module

#### J1

No.	Interface	Label	Explanation
1	J1-1/2	FAN	Interface of fan
2	J1-3/4	FANGND	Ground
3	J1-5	FAN_12V	12V working power supply of the fan
4	J1-6	FANSPD	Control signal of adjusting rotate speed of the fan
5	J1-7	FANDET	Sampling signal of fault for the fan

## 2.2 IGBT driving module (IGBTDR)

### 2.2.1 Introduction of principle of IGBT driving module

IGBT driving module adopts the structure of forward transformer, and the IC3845 works under effect of FAN12V, the output PWM wave controls on/off of MOS pipe. When the MOS pipe is on, energy in edge of transformer will be transformed to all secondary edges which will produce needed power supply to provide it to optical coupling chip 316J. the 316J can get the PWM output wave (average of high level is +15V and average low level is -10V) with positive and negative poles, which has the same pulse width and frequency with outer PWM wave, by effect of outer output PWM wave to drive the IGBT pipe. When the voltage detected by VEC over-current protection is high to 7V due to over-current among CE poles of IGBT pipe, the 316J will produce VCE protective warning FAULT signal t once and turn off the driving output signal to protect the IGBT.

### 2.2.2 Schematic circuit and physical map of IGBT driving module



Figure 2.2.1 Physical Map of IGBT Driving Module

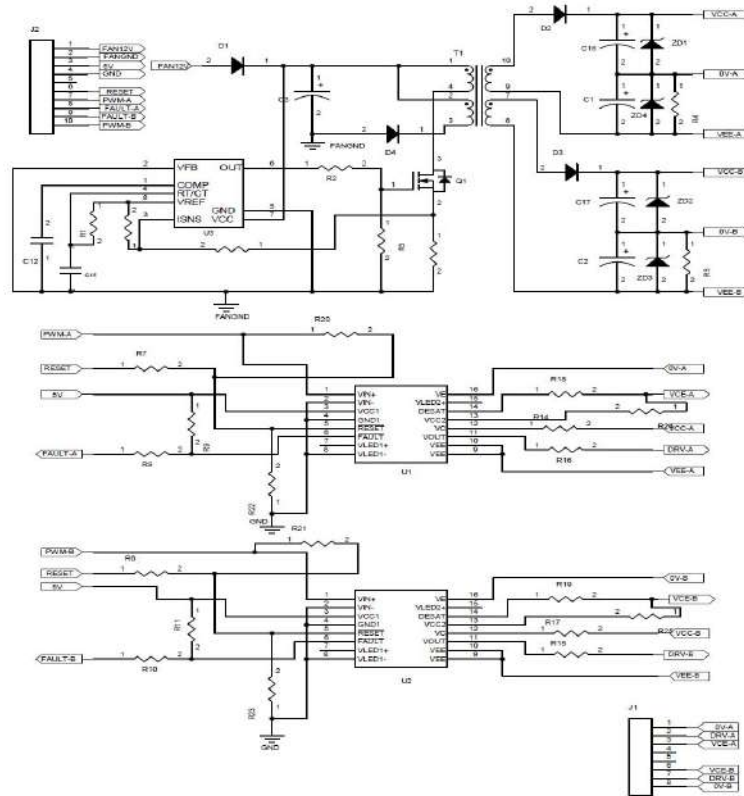


Figure 2.2.2 Schematic Circuit of IGBT Driving Module

### 2.2.3 Explanation for signal interface of IGBT driving module

#### J2

No.	Interface	Label	Explanation
1	J2-1	FAN12V	Input 12V power supply of the fan
2	J2-2	FANGND	Input ground of the power supply
3	J2-3	5V	Input DC 5V power supply
4	J2-4	GND	Input corresponding ground of DC 5V
5	J2-6	RESET	Reset pin
6	J2-7	PWM-A	Input PWM control signal A
7	J2-8	FAULT-A	VCE-A protective warning signal
8	J2-9	FAULT-B	VCE-B protective warning signal
9	J2-10	PWM-B	Input PWM control signal B

#### J1

No.	Interface	Label	Explanation
1	J2-1	0V-A	Input reference ground of PWM driving signal A
2	J2-2	DRV-A	Output PWM driving signal A
3	J2-3	VCE-A	IGBT VCE sampling A
5	J2-6	VCE-B	IGBT VCE sampling B
6	J2-7	DRV-B	Output PWM driving signal B
7	J2-8	0V-B	Output reference ground of PWM driving signal B



## 2.3 SCR driving module (SCRDRV)

### 2.3.1 Introduction of principle of SCR driving module

Main circuit of SCR driving module is the structure of FLYBACK transformer, the IC3845 working power supply is supplied by 12V power supply, the control signal STSON of SCR driving is in high level at the beginning, there is no PWM output for the IC3845, and there is also no output for the secondary edge of transformer. When the main control panel switches the STSON signal to low level, there is PWM output for IC3845 and the control switch is on and off. When MOS is on, original edge of transformer will store the energy; while when the MOS is off, energy stored by original edge of the transformer will be transferred to the secondary edge which will output two driving voltage sources to drive two SCR.

### 2.3.2 Schematic circuit and physical map of SCR driving module

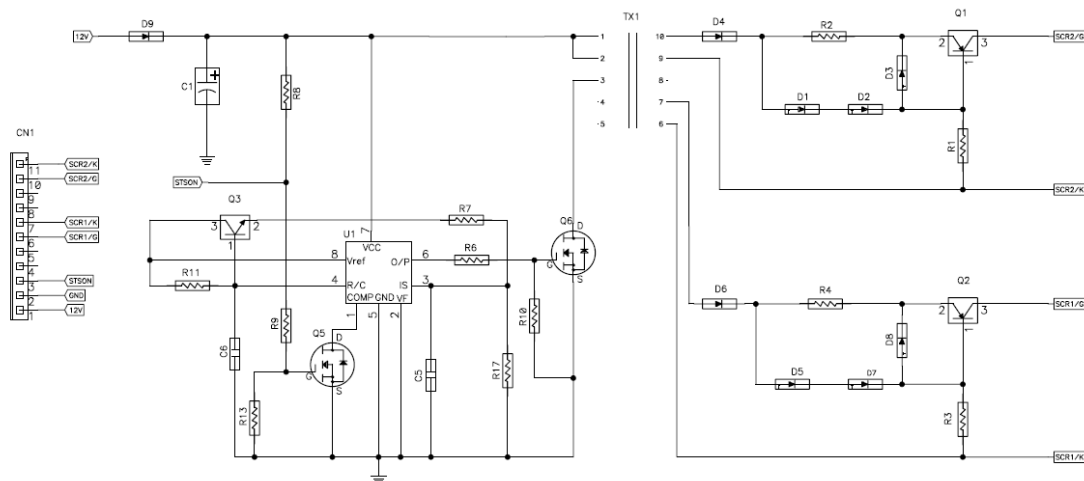


Figure 2.3.1 Schematic Circuit of SCR Driving Module

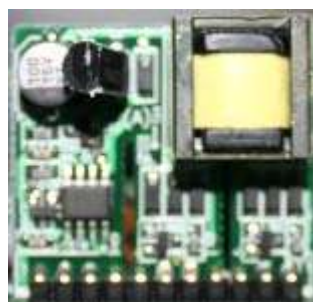


Figure 2.3.2 Physical Map of SCR Driving Module

### 2.3.3 Explanation for signal interface of SCR driving module

#### CN1

No.	Interface	Label	Explanation
1	CN1-1	12V	Input 12V DC source
2	CN1-2	GND	Input ground
3	CN1-3	STSON	Input signal of SCR driving

4	CN1-6	SCR1/G	The first driving output positive
5	CN1-7	SCR1/K	The first driving output negative
6	CN1-10	SCR2/G	The second driving output positive
7	CN1-11	SCR2/K	The second driving output negative

## 2.4 Auxiliary power supply module (SPS)

### 2.4.1 Introduction of principle of SPS

Structure of main circuit of SPS is the structure of FLYBACK transformer. After pressing button of power on after the main power is supplied under main power mode or battery mode, the IC3845 will build a working power supply and start to work, and the driving output pin will output PWM wave form to drive the MOS pipe. When MOS pipe is on, original edge of transformer will store the energy and there is no output for the secondary edge; when MOS pipe is off, energy of transformer will be transferred to all circuits of secondary edge to produce  $\pm 15V$ ,  $+12V$ ,  $+5V$  and FAN12V power supply to supply needed working power supply for the whole UPS system.

### 2.4.2 Schematic circuit and physical map of SPS

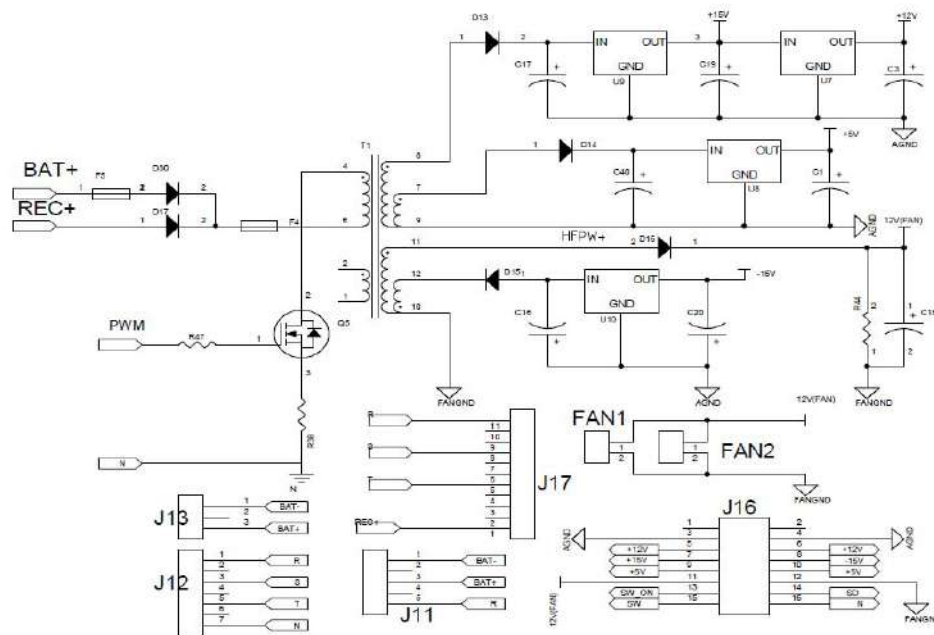


Figure 2.4.1 Schematic Circuit of SPS



Figure 2.4.2 Physical Map of SPS

### 2.4.3 Explanation for signal interface of SPS

#### J11

No.	Interface	Label	Explanation
1	J11-1	BAT-	Supply negative voltage of battery to SOFTSTART plate
2	J11-3	BAT+	Supply positive voltage of battery to SOFTSTART plate
3	J11-5	R	Supply Phase R of main power input for SOFTSTART plate

#### J12

No.	Interface	Label	Explanation
1	J12-1	R	Phase R of main power input
2	J12-3	S	Phase S of main power input
3	J12-5	T	Phase T of main power input
4	J12-7	N	N cable of main power input

#### J13

No.	Interface	Label	Explanation
1	J13-1	BAT-	Battery negative
2	J13-3	BAT+	Battery positive

#### J16

No.	Interface	Label	Explanation
1	J16-3/4	AGND	Corresponding grounds of output $\pm 15V$ , $+12V$ and $+5V$
2	J16-5/6	+12V	Output DC $+12V$
3	J16-7	+15V	Output DC $+15V$
4	J16-8	-15V	Output DC $-15V$
5	J16-9/10	+5V	Output DC $+5V$
6	J16-11	12V(FAN)	Output $12V$ DC used to supply power to the fan
7	J16-12	FANGND	Output ground used to supply power the fan
8	J16-13	SW_ON	Power signal (used for single module debugging)
9	J16-14	SD	SPS can be stopped by this signal

10	J16-15	SW	Control signal of SPS start
11	J16-16	N	Original edge ground of SPS

### **J17**

No.	Interface	Label	Explanation
1	J17-1	REC+	Rectified positive voltage after rectified by SPS-REC small plate
2	J17-5	T	Phase T of main power
3	J17-8	S	Phase S of main power
4	J17-11	R	Phase R of main power

### **FAN1/ FAN2**

No.	Interface	Label	Explanation
1	FAN1-1/ FAN2-1	12V(FAN)	12V DC outputted to the fan
2	FAN1-2/ FAN2-2	FANGND	Ground outputted to the fan

## **2.5 Soft start module (SOFTSTART)**

### **2.5.1 Introduction of principle of SOFTSTART**

When DSP receives the power signal, it will send the signal of soft start to SOFTSTART module, the relay will be closed, and Phase R of main power or battery will charge the positive and negative BUS after rectification to charge the BUS capacity before starting of PFC circuit. The soft start process will be finished and SOFTSTART module stops working after certain voltage value is boosted for the BUS voltage.

### **2.5.2 Schematic circuit and physical map of SOFTSTART**

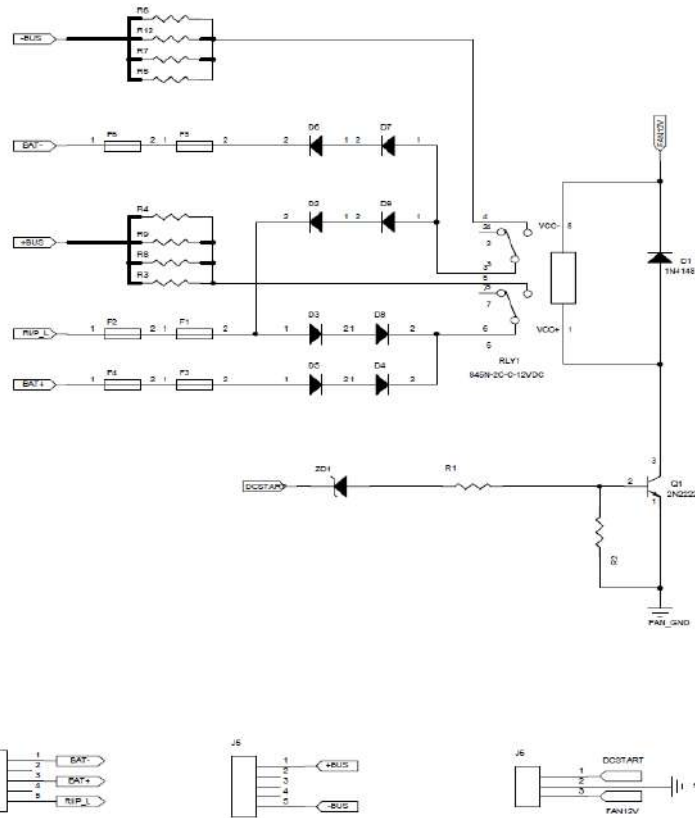


Figure 2.5.1 Schematic Circuit of SOFTSTART

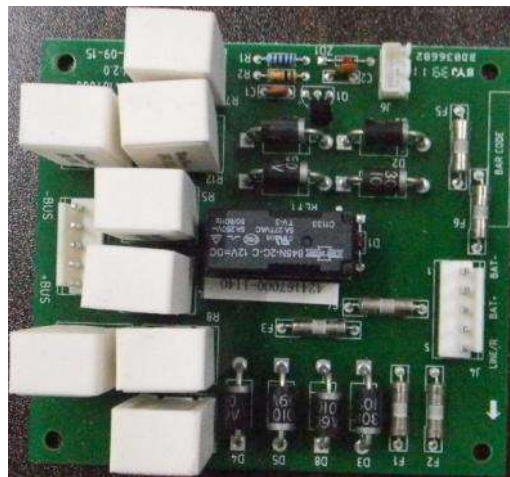


Figure 2.5.2 Physical Map of SOFTSTART

### 2.5.3 Explanation for signal interface of SOFTSTART

#### J4

No.	Interface	Label	Explanation
1	J4-1	BAT-	Input battery negative
2	J4-3	BAT+	Input battery positive
3	J4-5	R/P_L	Input phase R of main power

#### J5

No.	Interface	Label	Explanation
1	J5-1	+BUS	+BUS outputted to LC board
2	J5-5	-BUS	-BUS outputted to LC board

### J6

No.	Interface	Label	Explanation
1	J6-1	DCSTART	Switch control signal of SOFTSTART
2	J6-2	FAN_GND	Ground of 12V power supply of the fan
3	J6-3	FAN12V	12V power supply of the fan

## 2.6 Input board (IP-BOARD)

### 2.6.1 Introduction of functions of IP-BOARD

IP-BOARD mainly achieves over-current protection of main power and batter input and sampling of main power, battery and bypass voltage.

### 2.6.2 Schematic circuit and physical map of IP-BOARD

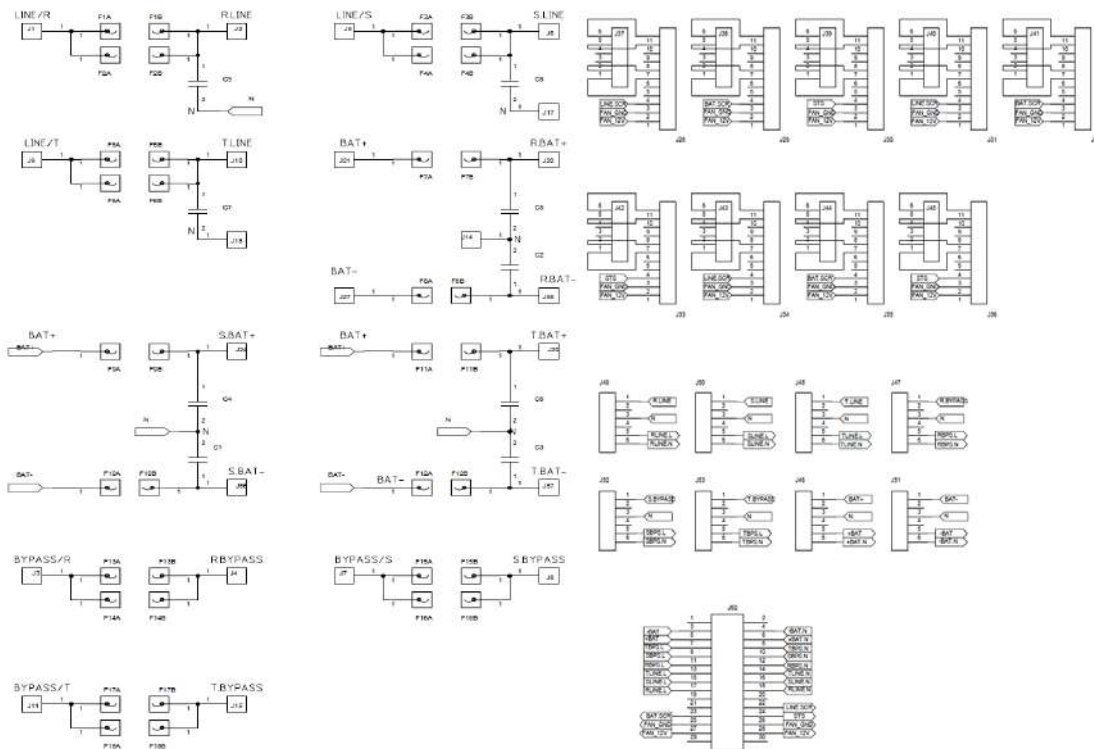


Figure 2.6.1 Schematic Circuit of IP-BOARD

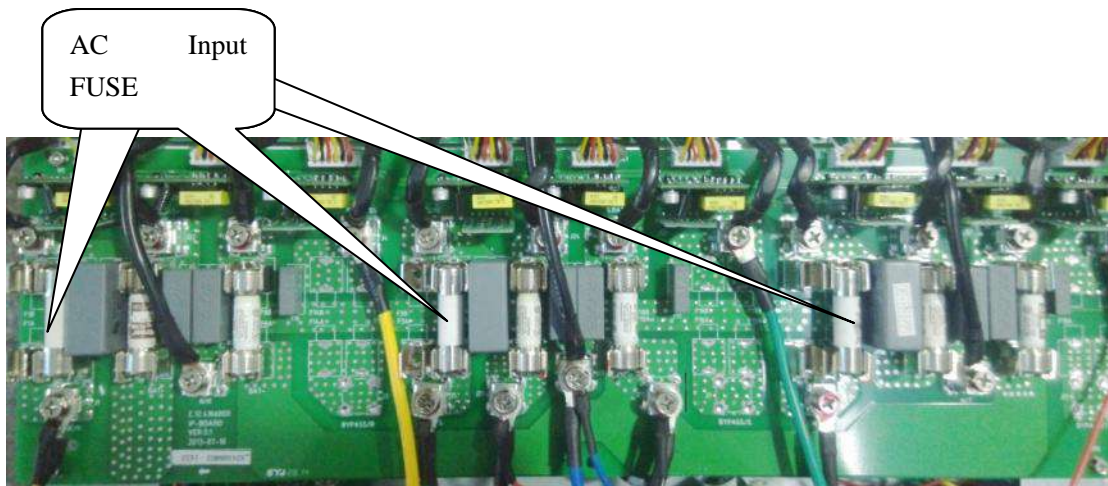


Figure 2.6.2 Physical Map of IP-BOARD for 10KVA Power Module

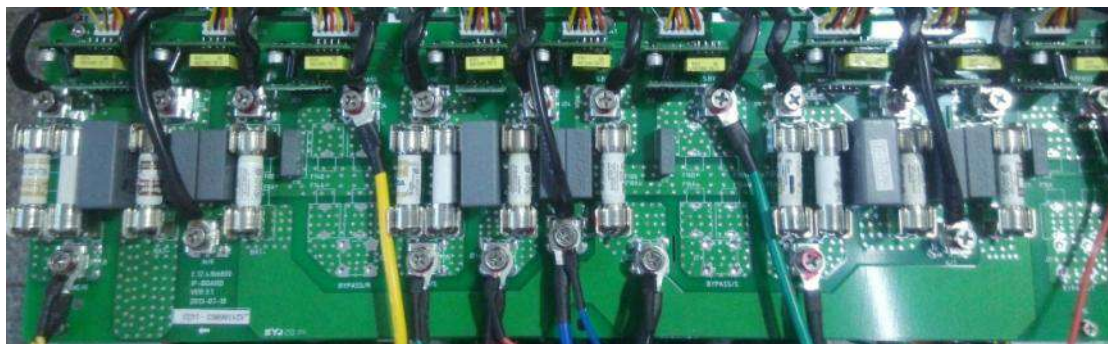


Figure 2.6.3 Physical Map of IP-BOARD for 20KVA and 30KVA Power Module

The difference between IP-BOARD of 10K,20K,and 30K power module,detail below the Chart

Power module capacity	Number of AC input FUSE per phase
10KVA	1
20KVA	2
30KVA	2

Chart 2.6.1 The difference between two types of IP\_Board

### 2.6.3 Explanation for signal interface of IP-BOARD

**J37-J45** (J37, J40 and J43 match with main power SCR of R, S and Phase T of rectifying plate respectively; J39, J42 and J45 match with bypass SCR of R, S and Phase T of bypass SCR module)

No.	Interface	Label	Explanation
1	1	SCR1/G	The first output positive of SCR driving
2	2	SCR1/K	The first output negative of SCR driving
3	5	SCR2/G	The second output positive of SCR driving
4	6	SCR2/K	The second output negative of SCR driving

#### **J60**

No.	Interface	Label	Explanation
1	J60-3/4	-BAT;-BAT.N	Voltage sampling signal of negative battery
2	J60-5/6	+BAT;+BAT.N	Voltage sampling signal of positive battery
3	J60-7/8	TBPS.L;TBPS.N	Voltage sampling signal of Phase T bypass
4	J60-9/10	SBPS.L;SBPS.N	Voltage sampling signal of Phase S bypass
5	J60-11/12	RBPS.L;RBPS.N	Voltage sampling signal of Phase R bypass

6	J60-13/14	TLINE.L;TLINE.N	Voltage sampling signal of Phase T main power
7	J60-15/16	SLINE.L;SLINE.N	Voltage sampling signal of Phase S main power
8	J60-17/18	RLINE.L;RLINE.N	Voltage sampling signal of Phase R main power
9	J60-22	LINE.SCR	Driving control signal of main power SCR driving module
10	J60-23	BAT.SCR	Driving control signal of battery SCR driving module
11	J60-24	STS	Driving control signal of bypass SCR driving module
12	J60-25/26	FAN_GND	Ground of 12V power supply of the fan
13	J60-27/28	FAN_12V	12V power supply input of the fan

## 2.7 Rectifier module (RECTIFIER)

### 2.7.1 Introduction of principle of RECTIFIER module

RECTIFIER module is mainly composed by main power SCR which is used to rectify the input main power into DC voltage and battery SCR which is used to control disconnection of battery input.

### 2.7.2 Schematic circuit and physical map of RECTIFIER module

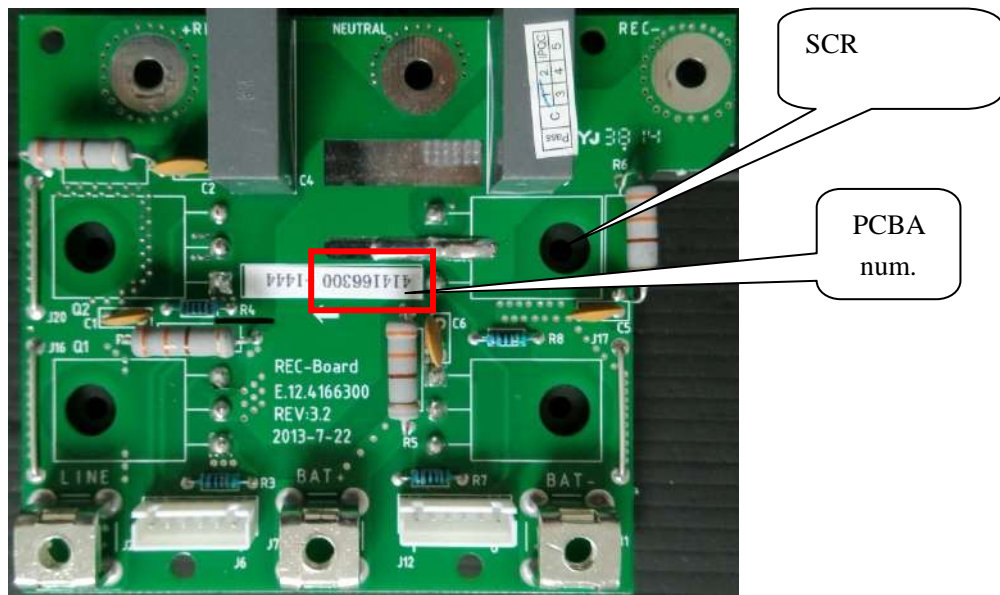


Figure 2.7.1 Physical Map of RECTIFIER Module

The difference between RECTIFIER of 10K,20K,and 30K power module, detail below the Chart

Power module capacity	Type of SCR	PCBA number
10KVA	IR_40TPS12APBP(35A1200V)	414166302
20KVA	CLA 50E 1200HB (50A 1200V)	414166300
30KVA	CLA 50E 1200HB (50A 1200V)	414166300



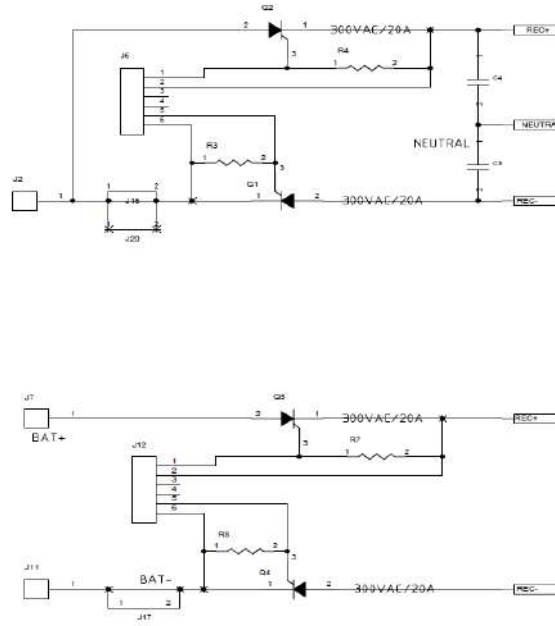


Figure 2.7.2 Schematic Circuit of RECTIFIER Module

### 2.7.3 Explanation for signal interface of RECTIFIER module

#### J2

No.	Interface	Label	Explanation
		LINE	Input terminal of main power

#### J7

No.	Interface	Label	Explanation
		BAT+	Battery positive

#### J11

No.	Interface	Label	Explanation
		BAT-	Battery negative

#### J6/J12

No.	Interface	Label	Explanation
1	J6/J12 -1	SCR1/G	The first output positive of SCR driving
2	J6/J12 -2	SCR1/K	The first output negative of SCR driving
3	J6/J12 -5	SCR2/G	The second output positive of SCR driving
4	J6/J12 -6	SCR2/K	The second output negative of SCR driving

## 2.8 Bypass SCR module (BPS-SCR)

### 2.8.1 Introduction of bypass SCR module

Bypass SCR module plays the role of switch control under bypass mode.

### 2.8.2 Schematic circuit and physical map of bypass SCR module

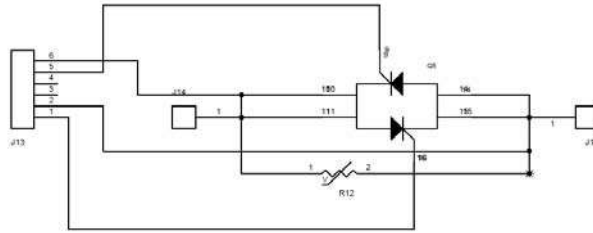


Figure 2.8.1 Schematic Circuit of Bypass SCR Module



Figure 2.8.2 Physical Map of Bypass SCR Module

### 2.8.3 Explanation for signal interface of bypass SCR module

#### J13

No.	Interface	Label	Explanation
1	J13-1	SCR1/G	The first output positive of SCR driving
2	J13-2	SCR1/K	The first output negative of SCR driving
3	J13-5	SCR2/G	The second output positive of SCR driving
4	J13-6	SCR2/K	The second output negative of SCR driving

#### J14

No.	Interface	Label	Explanation
		BYP	Input terminal of bypass

#### J15

No.	Interface	Label	Explanation
		BPS	BPS bypass terminal connected to output board

## 2.9 Power factor correction module (PFC)

### 2.9.1 Introduction of circuit principle of PFC

Circuit of power factor correction is composed by PFC inductance and BUS capability in PFC board and LC board.

Working principle of PFC board:

PFC circuit mainly is composed by boost circuit, and the IGBT pipe will be on/off under control of PWM driving. When the IGBT is on, PFC inductance will store the energy, and BUS capability supplies power to backward; when the IGBT is off, the diode is on, induced electromotive force of inductance is in series connection with input rectified voltage to output constant BUS voltage and supply power to BUS capability.

At the same time, DSP inputs voltage and PFC inductance current by sampling, treated by DSP arithmetic circuit, adjusts IGBT pipe to drive PWM wave form so that the wave form of input current is the same with wave form of rectified voltage and the input power factor of UPS is

improved.

### 2.9.2 Schematic circuit and physical map of PFC module

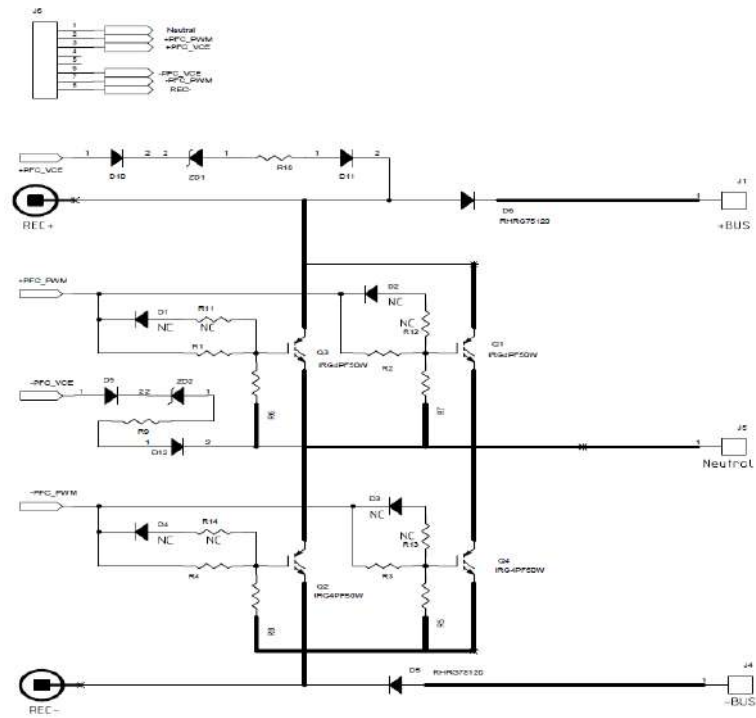


Figure 2.91 Schematic Circuit of PFC Module



Figure 2.9.2 Physical Map of PFC Module for 10KVA Power Module

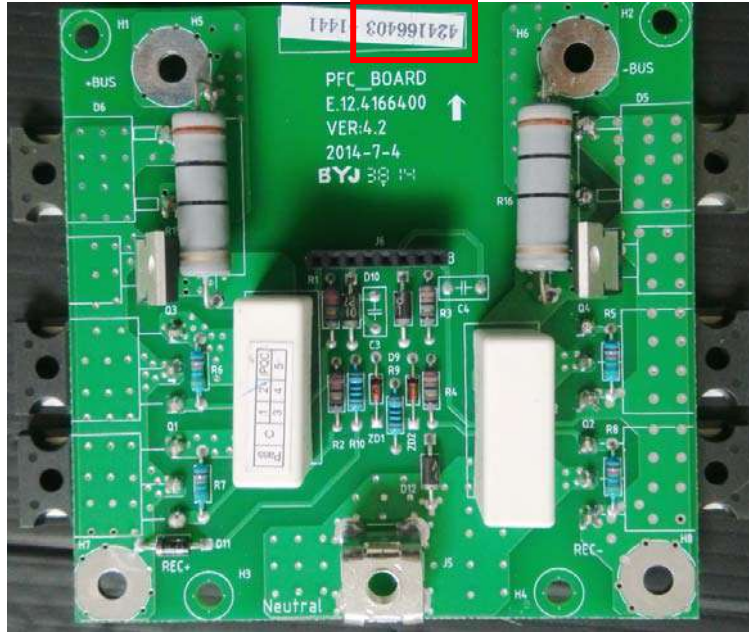


Figure 2.9.3 Physical Map of PFC Module for 30KVA Power Module

The difference between the PFC circuit of 10KVA,20KVA,and 30KVA power module

Power capacity	Module	The IGBT for PFC	The number of PFC IGBT per phase	PCBA num.
10KVA		IGBT,FGH40T100SMD(1000V 40A)	2	424166402
20KVA		IGBT,FGH40T100SMD(1000V 40A)	4	424166403
30KVA		IGBT,IKW40N120H3,(1200V,40A)	4	424166401

### 2.9.3 Explanation for signal interface of PFC module

**J6** (matching with J1 of IGBTDR module)

No.	Interface	Label	Explanation
1	J6-1	Neutral	Reference ground of PWM driving signal of IGBT in positive side
2	J6-2	+PFC_PWM	PWM driving signal of IGBT in positive side
3	J6-3	+PFC_VCE	VCE sampling of IGBT in positive side
4	J6-6	-PFC_VCE	VCE sampling of IGBT in negative side
5	J6-7	-PFC_PWM	PWM driving signal of IGBT in negative side
6	J6-8	REC-	Reference ground of PWM driving signal of IGBT in negative side

## 2.10 Inverter module (INVERTER)

### 2.10.1 Introduction of circuit principle of INVERTER

INVERTER module, inverter inductance in LC board and inverter output capability in output board compose the inverter circuit of UPS, it is the half-bridge structure. The upper and lower half-bridge IGBT takes action of on/off under control of PWM driving, filtered by LC, and then the inverter sinusoidal wave output can be obtained.

### 2.10.2 Schematic circuit and physical map of INVERTER module

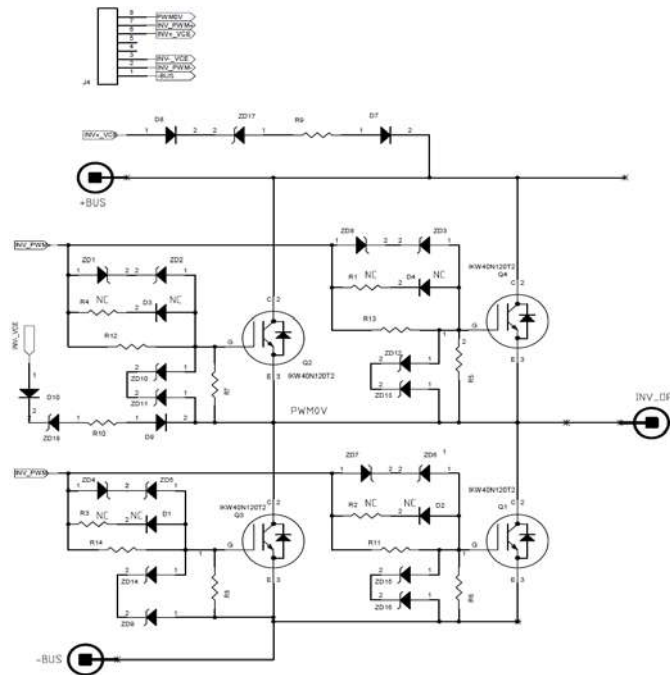


Figure 2.10.1 Schematic Circuit of INVERTER Module

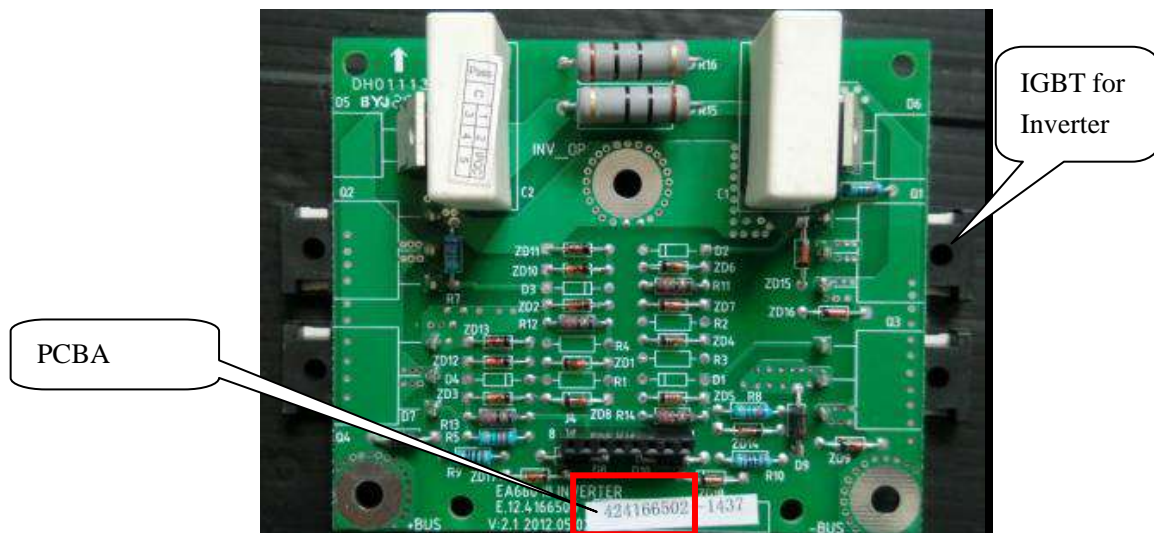


Figure 2.10.2 Physical Map of INVERTER Module for 30KVA Power Module

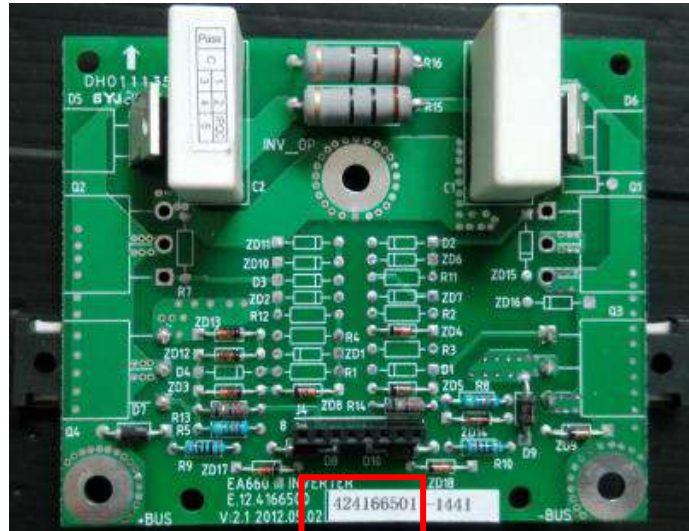


Figure 2.10.3 Physical Map of INVERTER Module for 10KVA Power Module

The difference between the INVERTER circuit of 10KVA,20KVA,and 30KVA power module

Power Module Capacity	IGBT for Inverter	PCBA num.	Quantity per phase
10KVA	IGBT,IKW40N120H3,(1200V,40A)	424166501	2PCS
20KVA	IGBT,IKW40N120H3,(1200V,40A)	424166500	4PCS
30KVA	IGBT,IKW40N120H3,(1200V,40A)	424166502	4PCS

### 2.10.3 Explanation for signal interface of INVERTER module

**J4** (matching with J1 of IGBTDR module)

No.	Interface	Label	Explanation
1	J4-1	-BUS	Reference ground of PWM driving signal of IGBT in negative side
2	J4-2	INV_PWM-	PWM driving signal of IGBT in negative side
3	J4-3	INV-_VCE	VCE sampling of IGBT in negative side
4	J4-6	INV+_VCE	VCE sampling of IGBT in positive side
5	J4-7	INV_PWM+	PWM driving signal of IGBT in positive side
6	J4-8	PWM0V	Reference ground of PWM driving signal of IGBT in positive side

## 2.11 Inductance capability board (LC-BOARD)

### 2.11.1 Introduction of functions of LC-BOARD

There are PFC, INV inductance, BUS electrolytic capacitor, and Hall sensor in the LC-BOARD, achieving the functions of PFC inductance current, INV inductance current, sampling of BUS voltage and speed adjustment of the fan.

### 2.11.2 Schematic circuit and physical map of LC-BOARD

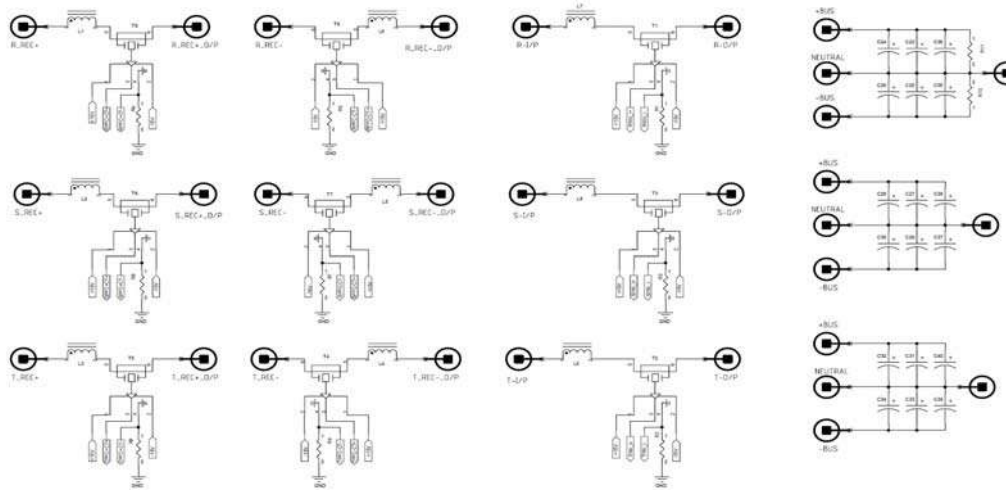


Figure 2.11.1 Schematic Circuit of LC-BOARD

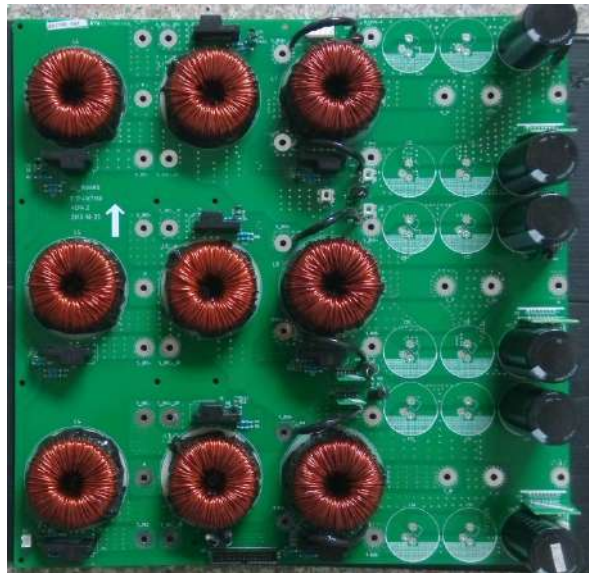


Figure 2.11.2 Physical Map of LC-BOARD for 10KVA Power Module

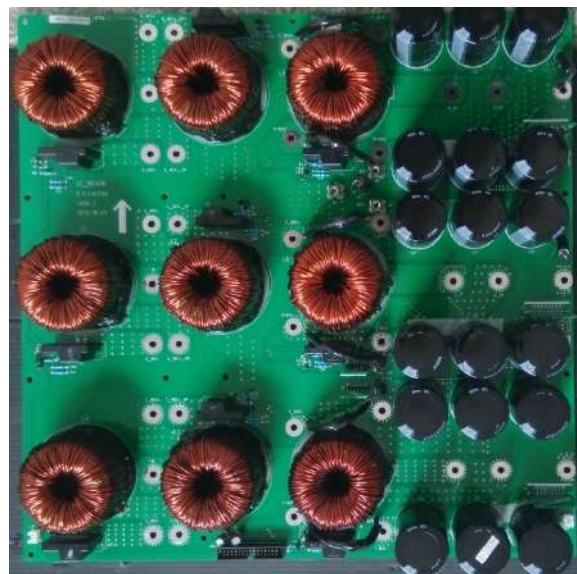


Figure 2.11.2 Physical Map of LC-BOARD for 20KVA and 30KVA Power Module

The difference between the LC-BOARD of 10KVA,20KVA,and 30KVA power module

	The number capacity	Fan drv	PCBA num.
10KVA	6pcs (450V,820uf)	3	424167103
20KVA	18pcs(450V.820uf)	6	424167104
30KVA	18pcs(450V,820uf)	6	424167102

### 2.11.3 Explanation for signal interface of LC-BOARD

#### J38

No.	Interface	Label	Explanation
1	J38-1/5	+BUS; - BUS	±BUS outlet pin, connected with soft start board J5

#### J54/J55/J56

No.	Interface	Label	Explanation
1	J54/J55/J56-1	FAN12V	Output 12V power supply of the fan
2	J54/J55/J56-2	FAN_1;FAN_2;FAN_3	Connecting pin of the fan

#### J63

No.	Interface	Label	Explanation
1	J63-1	GND	Ground
2	J63-2	+15V	Input +15V DC
3	J63-4	-15V	Input -15V DC
4	J63-5/6	TPFC-CT+;TPFC-CT-	PFC inductance current sampling in negative side of Phase T
5	J63-7/8	SPFC-CT+;SPFC-CT-	PFC inductance current sampling in negative side of Phase S
6	J63-9/10	RPFC-CT+;RPFC-CT-	PFC inductance current sampling in negative side of Phase R
7	J63-11/12	TPFC+CT+;TPFC+CT-	PFC inductance current sampling in positive side of Phase T
8	J63-13/14	SPFC+CT+;SPFC+CT-	PFC inductance current sampling in positive side of Phase S
9	J63-15/16	RPFC+CT+;RPFC+CT-	PFC inductance current sampling in positive side of Phase R
10	J63-17/18	RINV_I+; RINV_I-	INV current sampling in Phase R
11	J63-19/20	SINV_I+; SINV_I-	INV current sampling in Phase S
12	J63-21/22	TINV_I+; TINV_I-	INV current sampling in Phase T
13	J63-23/24	-BUS.V; -BUS.N	Negative BUS voltage sampling
14	J63-25/26	+BUS.V; +BUS.N	Positive BUS voltage sampling
15	J63-27	FANDET2	Sampling signal of fault of the fan 2
16	J63-28	FANSPEED	Control signal of rotate speed of the fan
17	J63-29	FANDET1	Sampling signal of fault of the fan 1
18	J63-30	FANDET0	Sampling signal of fault of the fan 0

#### J64



No.	Interface	Label	Explanation
1	J64-1	FAN12V	Output of 12V power supply of the fan
2	J64-2	FAN_GND	Ground of 12V power supply of the fan

## 2.12 IGBT connecting plate (IGBT-CONNECTOR)

### 2.12.1 Introduction of functions of IGBT-CONNECTOR

IGBT-CONNECTOR plays role of connecting the main control panel and IGBT driving module, mainly achieves functions of PWM signal inversion of main control panel, IGBT over-current alarm detection, IGBT driving interlocking of inverter upper and lower half-bridge, and temperature sampling of radiator.

### 2.12.2 Schematic circuit and physical map of IGBT-CONNECTOR

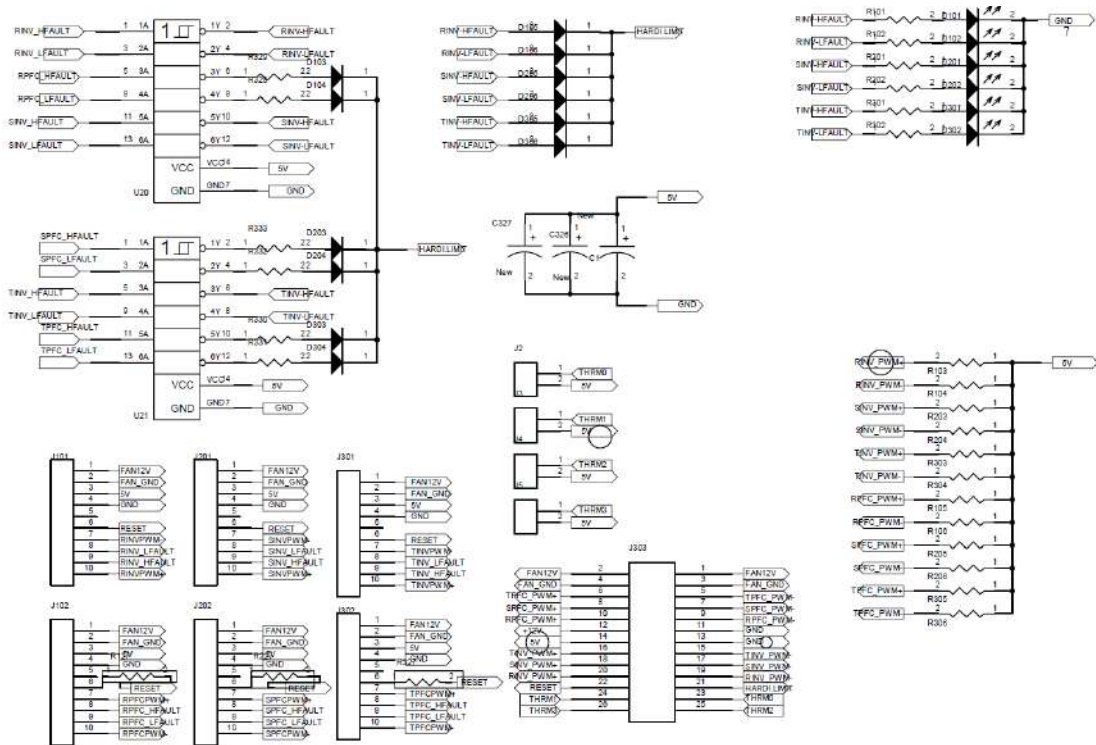


Figure 2.12.1 Schematic Circuit of IGBT-CONNECTOR

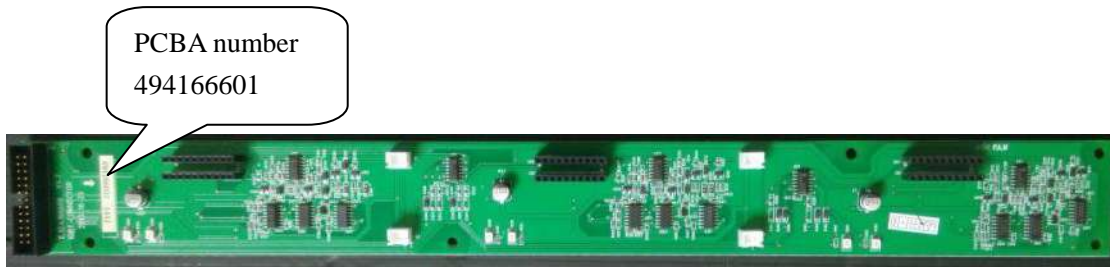


Figure 2.12.2 Physical Map of IGBT-CONNECTOR

### 2.12.3 Explanation for signal interface of IGBT-CONNECTOR

#### J101/J201/J301 (matching with J2 of IGBTDR module)

No.	Interface	Label	Explanation
1	J101-1	FAN12V	Input 12V power supply of the fan
2	J101-2	FAN_GND	Input power supply ground of the fan
3	J101-3	5V	Input DC 5V power supply
4	J101-4	GND	Input DC 5V corresponding ground
5	J101-6	RESET	Reset pin
6	J101-7	RINVPWM-	Signal of driving board inputted to IGBT in INV negative side of phase R
7	J101-8	RINV_LFAULT	FAULT signal of IGBTDR module in INV negative side of phase R
8	J101-9	RINV_HFAULT	FAULT signal of IGBTDR module in INV positive side of phase R
9	J101-10	RINVPWM+	Signal of driving board outputted to IGBT in INV positive side of phase R

#### J102/J202/J302 (matching with J2 of IGBTDR module)

No.	Interface	Label	Explanation
1	J102-1	FAN12V	12V power supply of the fan
2	J102-2	FAN_GND	12V power supply ground of the fan
3	J102-3	5V	DC 5V power supply
4	J102-4	GND	DC 5V corresponding ground
5	J102-6	RESET	Reset pin
6	J102-7	RPFCPWM+	Signal outputted to IGBT driving board in PFC positive side of phase R
7	J102-8	RPFC_HFAULT	FAULT signal of IGBTDR module in PFC positive side of phase R
8	J102-9	RPFC_LFAULT	FAULT signal of IGBTDR module in PFC negative side of phase R
9	J102-10	RPFCPWM-	Signal outputted to IGBT driving board in PFC negative side of phase R

#### J303

No.	Interface	Label	Explanation
1	J303-1/2	FAN12V	Input 12V power supply of the fan
2	J303-3/4	FAN_GND	Input 12V power supply ground of the fan
3	J303-5/6	TPFC_PWM-; TPFC_PWM+	Pulse signal controlling PFC IGBT driving module in phase T
4	J303-7/8	SPFC_PWM-; SPFC_PWM+	Pulse signal controlling PFC IGBT driving module in phase S
5	J303-9/10	RPFC_PWM-; RPFC_PWM+	Pulse signal controlling PFC IGBT driving module in phase R
6	J303-11/13	GND	Corresponding ground of DC 12V and 5V

7	J303-12	12V	Input DC 12V power supply
8	J303-14	5V	Input DC 5V power supply
9	J303-15/16	TINV_PWM-; TINV_PWM+	Pulse signal controlling INV IGBT driving module in phase T
10	J303-17/18	SINV_PWM-; SINV_PWM+	Pulse signal controlling INV IGBT driving module in phase S
11	J303-19/20	RINV_PWM-; RINV_PWM+	Pulse signal controlling INV IGBT driving module in phase R
12	J303-21	HARDI.LIMIT	FAULT signal of IGBTDR module
13	J303-22	RESET	Reset control pin of IGBTDR module
14	J303-23/24/25/26	THRM0; THRM1; THRM2; THRM3	Temperature sampling signal

**J2/J3/J4/J5**

No.	Interface	Label	Explanation
1	J2-1/J3-1/J4-1/J5-1	THRM0; THRM1; THRM2; THRM3	Temperature sampling signal
2	J2/J3/J4/J5-2	5V	DC 5V power supply

**2.13 Output board (OP-BOARD)**

**2.13.1 Introduction of functions of OP-BOARD**

OP-BOARD mainly achieves sampling of output voltage current and inverter voltage as well as inverter voltage DC component and switch control of inverter output.

**2.13.2 Schematic circuit and physical map of OP-BOARD**

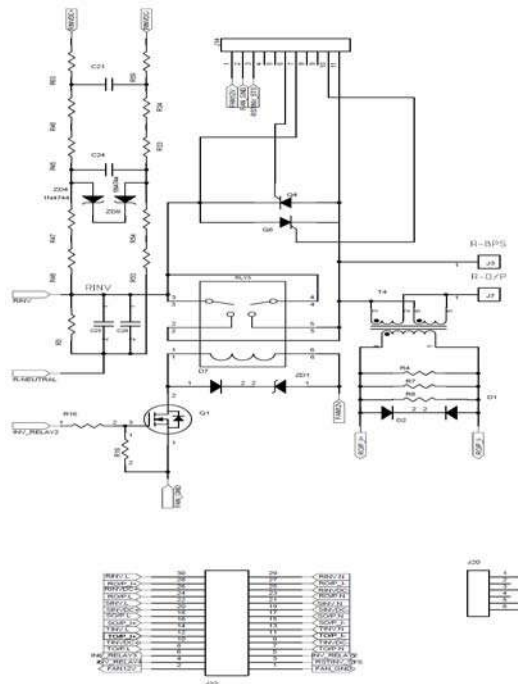


Figure 2.13.1 Schematic Circuit of OP-BOARD

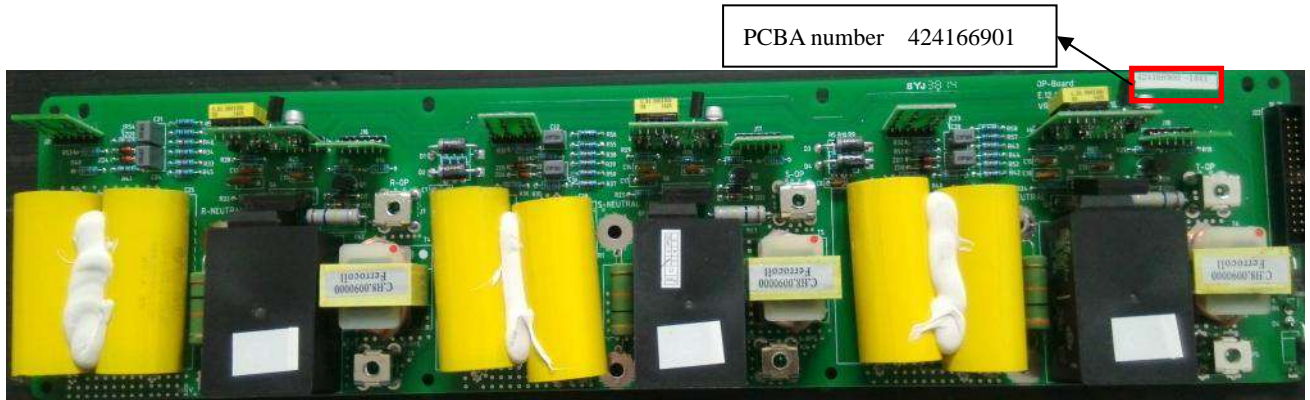


Figure 2.13.2 Physical Map of OP-BOARD for 30KVA Power Module

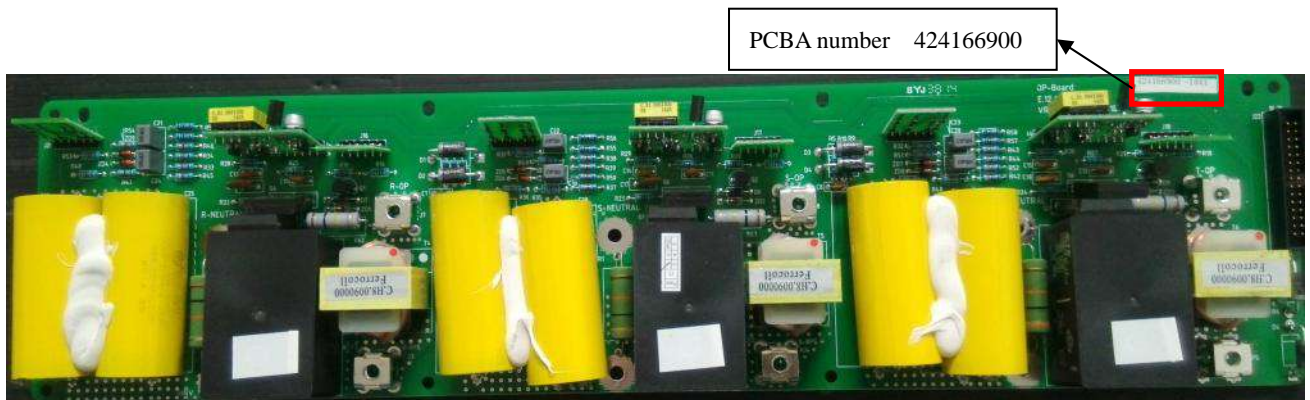


Figure 2.13.3 Physical Map of OP-BOARD for 10KVA and 20KVA Power Module

### 2.13.3 Explanation for signal interface of OP-BOARD

#### J22

No.	Interface	Label	Explanation
1	J22-1	FAN_GND	12V power supply ground of the fan
2	J22-2	FAN_12V	12V power supply input of the fan
3	J22-3	RSTINV_STS	Control signal of SCR driving module of inverter output
4	J22-4	INV_RELAY4	Control signal of inverter relay switch in phase T
5	J22-5	INV_RELAY2	Control signal of inverter relay switch in phase R
6	J22-6	INV_RELAY3	Control signal of inverter relay switch in phase S
7	J22-7/8	TO/P.N;TO/PL	Output voltage sampling in phase T
8	J22-9/10	TINVDC-;TINVDC+ C+	Inverter DC component sampling in phase T
9	J22-11/12	TO/P_I-;TO/P_I+	Output current sampling in phase T
10	J22-13/14	TINV.N;TINV.L	Inverter voltage sampling in phase T
11	J22-15/16	SO/P_I-;SO/P_I+	Output current sampling in phase S
12	J22-17/18	SO/P.N;SO/PL	Output voltage sampling in phase S
13	J22-19/20	SINVDC-;SINVDC+ C+	Inverter DC component sampling in phase S

14	J22-21/22	SINV.N;SINV.L	Inverter voltage sampling in phase S
15	J22-23/24	RO/P.N;RO/P.L	Output voltage sampling in phase R
16	J22-25/26	RINVDC-;RINVD C+	Inverter DC component sampling in phase R
17	J22-27/28	RO/P_I-;RO/P_I+	Output current sampling in phase R
18	J22-29/30	RINV.N;RINV.L	Inverter voltage sampling in phase S

## 2.14 Output filter board (OP\_EMI)

### 2.14.1 Schematic circuit and physical map of output filter board

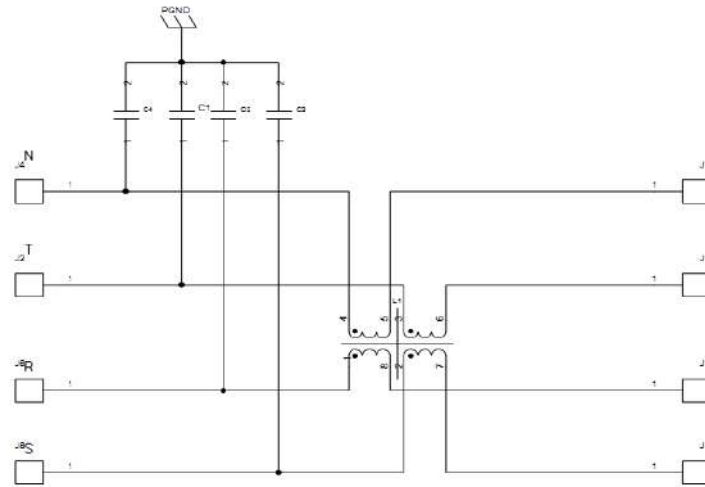


Figure 2.14.1 Schematic Circuit of OP\_EMI

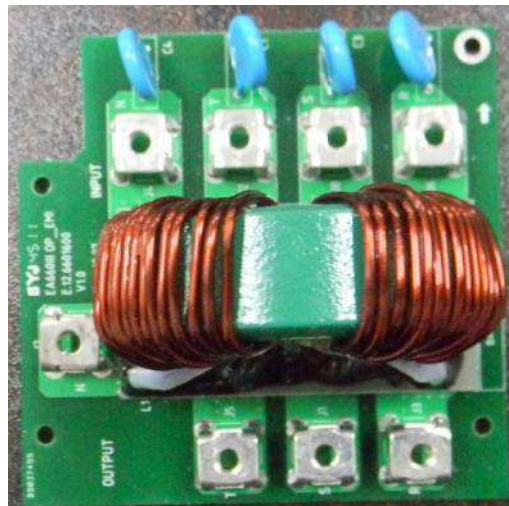


Figure 2.14.2 Physical Map of OP\_EMI

### 2.14.2 Explanation for signal interface of output filter board

No.	Interface	Label	Explanation
1	J6/J8/J2/J4	INPUT R/S/T/N	Output R/S/T/N of filter board
2	J3/J1/J5/J7	OUTPUT R/S/T/N	Output R/S/T/N of filter board

## 2.15 Power socket connecting plate (IN\_CON\_Z)

### 2.15.1 Schematic circuit and physical map of IN\_CON\_Z

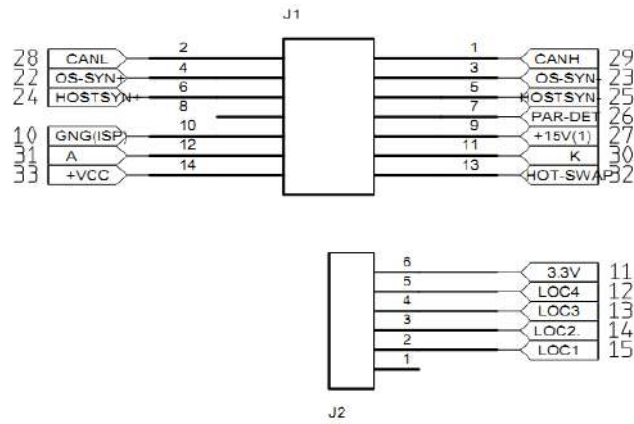


Figure 2.15.1 Schematic Circuit of IN\_CON\_Z

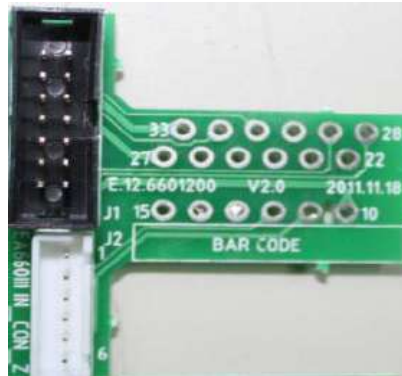


Figure 2.15.2 Physical Map of IN\_CON\_Z

### 2.15.2 Explanation of signal interface of IN\_CON\_Z

#### J1

No.	Interface	Label	Explanation
1	J1-1/2	CANH;CANL	CAN communication signal
2	J1-3/4	OS-SYN-; OS-SYN+	Synchronizing signal
3	J1-5/6	HOSTSYN-; HOSTSYN+	Synchronizing pulse signal
4	J1-7	PAR-DET	Sampling signal of disconnected line of parallel machine
5	J1-9	+15V( I )	Secondary side DC power supply +15V
6	J1-10	GNG(ISP)	Secondary side ground
7	J1-11	K	Corresponding ground of POWER_ON
8	J1-12	A	POWER_ON
9	J1-13	HOT-SWAP	Hot-plugging signal
10	J1-14	+VCC	Secondary side power supply

#### J2

No.	Interface	Label	Explanation

1	J2-2/3/4/5	LOC1; LOC2; LOC3; LOC4	Physical address sampling signal
2	J2-6	3.3V	DC 3.3V power supply

## 2.16 Power socket connecting plate (IN\_CON\_T)

### 2.16.1 Schematic circuit and physical map of IN\_CON\_T

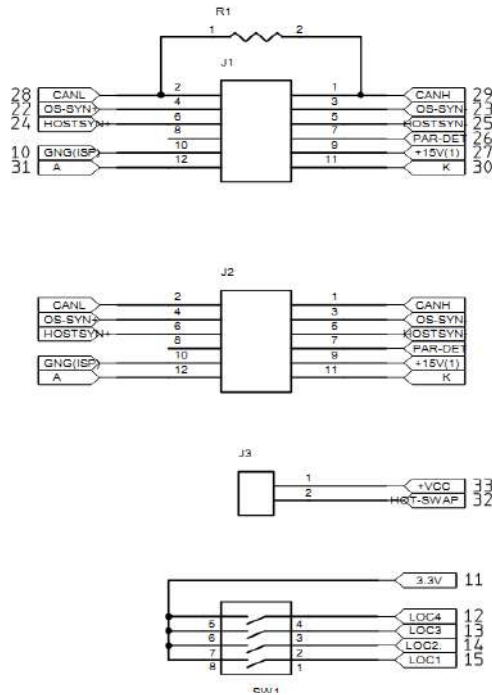


Figure 2.16.1 Schematic Circuit of IN\_CON\_T

### 2.16.2 Explanation for signal interface of IN\_CON\_T

#### J1/J2

No.	Interface	Label	Explanation
1	J1-1/2	CANH;CANL	CAN communication signal
2	J1-3/4	OS-SYN-; OS-SYN+	Synchronizing signal
3	J1-5/6	HOSTSYN-; HOSTSYN+	Synchronizing pulse signal
4	J1-7	PAR-DET	Sampling signal of disconnected line of parallel machine
5	J1-9	+15V(I)	Secondary side DC power supply +15V
6	J1-10	GNG(ISP)	Secondary side ground
7	J1-11	K	Corresponding ground of POWER_ON
8	J1-12	A	POWER_ON

#### J3

1	J3-1	+VCC	Secondary side power supply
2	J3-2	HOT-SWAP	Hot-plugging signal

## 2.17 Lamp Panel (POWER\_MODULE LED)

### 2.17.1 Introduction of functions of lamp panel

Lamp panel in front panel mainly achieves the functions of working power supply set indication, start status indication and fault warning of the module.

### 2.17.2 Schematic circuit and physical map of lamp panel

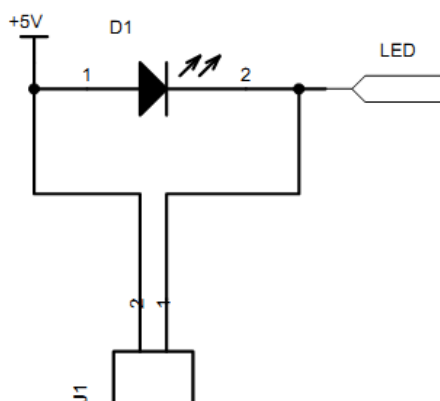


Figure 2.17.1 Schematic Circuit of Lamp Panel



Figure 2.17.2 Physical Map of Lamp Panel

### 2.17.3 Explanation for signal interface of lamp panel

#### J1

No.	Interface	Label	Explanation
1	J1-1	LED	Control signal of on/off of LED lamp
2	J1-2	+5V	+5V voltage supplied by main control panel

## 2.18 Control connecting plate (CNTL-CONNECTOR)

### 2.18.1 Introduction of functions of CNTL-CONNECTOR

CNTL-CONNECTOR mainly achieves the connection of signal interfaces of control panel, input and output board, power supply board, LC board, IGBT connecting plate, etc.

### 2.18.2 Schematic circuit and physical map of CNTL-CONNECTOR



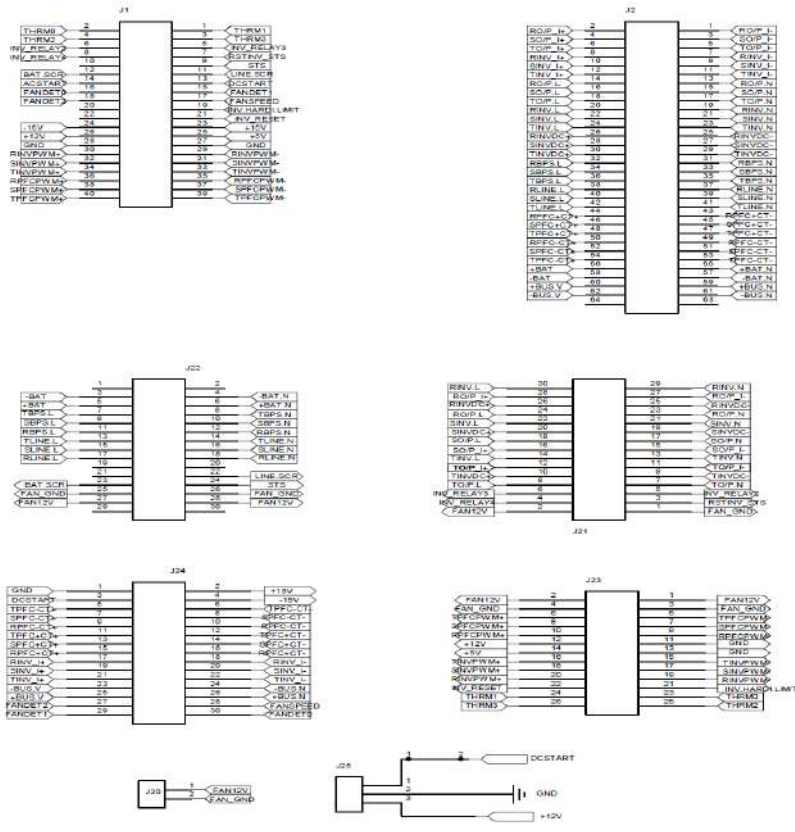


Figure 2.18.1 Schematic Circuit of CNTL-CONNECTOR

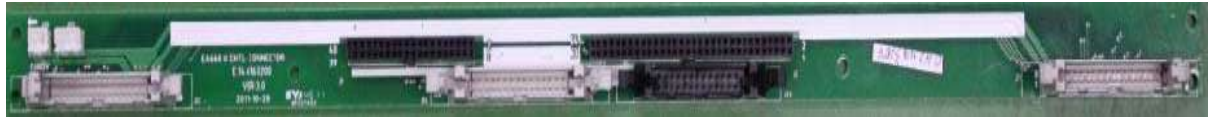


Figure 2.18.2 Physical Map of CNTL-CONNECTOR

2.18.3 Explanation for signal interface of CNTL-CONNECTOR

J1			
No.	Interface	Label	Explanation
1	J1-1/2/3/4	THRM1;THRM0; THRM3;THRM2	Temperature sampling signal
2	J1-5	INV_RELAY3	Control signal of inverter relay switch in phase S
3	J1-6	INV_RELAY2	Control signal of inverter relay switch in phase R
4	J1-7	RSTINVT_STS	Control signal of SCR driving signal of inverter output
5	J1-8	INV_RELAY4	Control signal of inverter relay switch in phase T
6	J1-9	STS	Control signal of bypass SCR
7	J1-11	LINE_SCR	SCR control signal of main power
8	J1-12	BAT_SCR	SCR control signal of battery
9	J1-13	DCSTART	Switch control signal of SOFTSTART
10	J1-15/16/18	FANDET1;FANDET0;	Sampling signal of fault of the fan

		FANDET2	
11	J1-17	FANSPEED	Control signal of rotate speed of the fan
12	J1-19	INV.HARDI.LIMIT	FAULT signal of IGBTDR module
13	J1-21	INV_RESET	Reset pin of IGBTDR module
14	J1-23/24/25/26	+15V;-15V; 5V ;12V	DC power supply
15	J1-27/28	GND	Ground
16	J1-29/30	RINVPWM-; RINVPWM+	Pulse signal controlling INV IGBTDR module in phase R
17	J1-31/32	SINVPWM-; SINVPWM+	Pulse signal controlling INV IGBTDR module in phase S
18	J1-33/34	TINVPWM-; TINVPWM+	Pulse signal controlling INV IGBTDR module in phase T
19	J1-35/36	RPFPCWM-; RPFPCWM+	Pulse signal controlling PFC IGBTDR module in phase R
20	J1-37/38	SPFPCWM-; SPFPCWM+	Pulse signal controlling PFC IGBTDR module in phase S
21	J1-39/40	TPFPCWM-; TPFPCWM+	Pulse signal controlling PFC IGBTDR module in phase T

## J2

No.	Interface	Label	Explanation
1	J2-1/2	RO/P_I-;RO/P_I+	Output current sampling in phase R
2	J2-3/4	SO/P_I-;SO/P_I+	Output current sampling in phase S
3	J2-5/6	TO/P_I-;TO/P_I+	Output current sampling in phase T
4	J2-7/8	RINV_I-; RINV_I+	INV current sampling in phase R
5	J2-9/10	SINV_I-; SINV_I+	INV current sampling in phase S
6	J2-11/12	TINV_I-; TINV_I+	INV current sampling in phase T
7	J2-13/14	RO/P.N;RO/P.L	Output voltage sampling in phase R
8	J2-15/16	SO/P.N;SO/P.L	Output voltage sampling in phase S
9	J2-17/18	TO/P.N;TO/P.L	Output voltage sampling in phase T
10	J2-19/20	RINV.N;RINV.L	Inverter voltage sampling in phase R
11	J2-21/22	SINV.N;SINV.L	Inverter voltage sampling in phase S
12	J2-23/24	TINV.N;TINV.L	Inverter voltage sampling in phase T
13	J2-25/26	RINVDC-;RINVDC+	Inverter DC component sampling in phase R
14	J2-27/28	SINVDC-;SINVDC+	Inverter DC component sampling in phase S
15	J2-29/30	TINVDC-;TINVDC+	Inverter DC component sampling in phase T
16	J2-31/32	RBPS.N;RBPS.L	Bypass voltage sampling signal in phase R
17	J2-33/34	SBPS.N;SBPS.L	Bypass voltage sampling signal in phase S
18	J2-35/36	TBPS.N;TBPS.L	Bypass voltage sampling signal in phase T
19	J2-37/38	RLINE.N;RLINE.L	Main power voltage sampling signal in phase R
20	J2-39/40	SLINE.N;SLINE.L	Main power voltage sampling signal in phase S
21	J2-41/42	TLINE.N;TLINE.L	Main power voltage sampling signal in phase T
22	J2-43/44	RPFC+CT-;RPFC+CT	PFC inductance current sampling in positive

		+	side of Phase R
23	J2-45/46	SPFC+CT-;SPFC+CT +	PFC inductance current sampling in positive side of Phase S
24	J2-47/48	TPFC+CT-;TPFC+CT +	PFC inductance current sampling in positive side of Phase T
25	J2-49/50	RPFC-CT-;RPFC-CT+	PFC inductance current sampling in negative side of Phase R
26	J2-51/52	SPFC-CT-;SPFC-CT+	PFC inductance current sampling in negative side of Phase S
27	J2-53/54	TPFC-CT-;TPFC-CT+	PFC inductance current sampling in negative side of Phase T
28	J2-55/56	+BAT.N;+BAT	Voltage sampling of positive battery
29	J2-57/58	-BAT.N;-BAT	Voltage sampling of negative battery
30	J2-59/60	+BUS.N;+BUS.V	Voltage sampling of positive BUS
31	J2-61/62	-BUS.N;-BUS.V	Voltage sampling of negative BUS

### J20

No.	Interface	Label	Explanation
1	J20-1	FAN12V	Input 12V power supply of the fan
2	J20-2	FAN_GND	Input 12V power supply ground of the fan

### J25

No.	Interface	Label	Explanation
1	J25-1	DCSTART	Switch control signal of SOFTSTART
2	J25-2	GND	Corresponding ground of DC 12V
3	J25-3	+12V	Input DC 12V power supply

### Interface matching

No.	Interface	Explanation
1	J21	Matching output board J22
2	J22	Matching input board J60
3	J23	Matching connecting plate J303 of IGBT
4	J24	Matching J63 of LC board

## 2.19 Control panel (CNTL)

### 2.19.1 Introduction of functions of CNTL

Transfer the analog signal received by connector of control panel into control signal output to control the UPS to work according to requirements under different conditions. 10-30KVA power module shared a control panel, and can set by a jumper in the CN4.

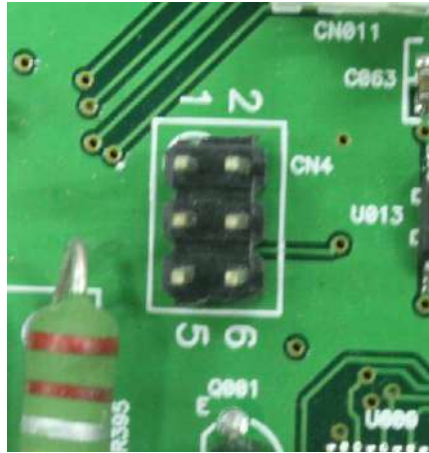


Figure2.19.1

CN4	1,2 pin	3, 4pin	5,6pin
10KVA	Short connect		
15KVA		Short connect	
20KVA			
30KVA			Short connect

### 2.19.2 Physical map of CNTL

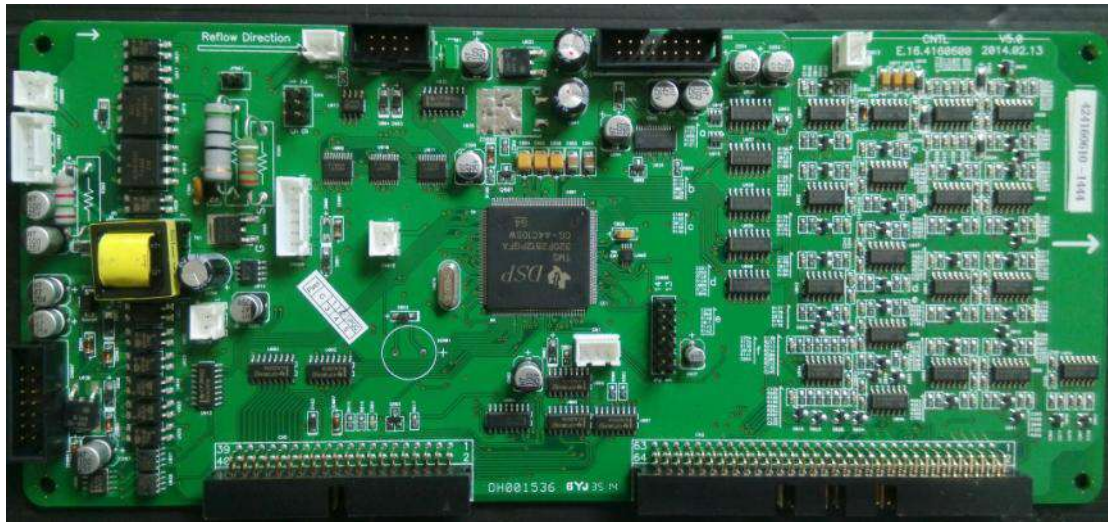


Figure 2.19.2 Physical Map of CNTL

### 2.19.3 Explanation for signal interface of CNTL

#### Interface matching

No.	Interface	Explanation
1	CN2	Matching control connecting plate J1
2	CN5	Matching control connecting plate J2
3	CN803	Matching SPS J16
4	CN007	Matching IN_CON_Z board J1
5	CN005	Matching IN_CON_Z board J2
6	CN012	Matching LED lamp panel J1 in front panel

**CN002**

CN002-1/2/ 3	IPOMSRXD;IPOMSTXD;GN D-S	Communication interface of serial port of single module
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**CN011**

CN011-1/2	N; SW	Connect with button of power on of single module, pressing it for 5s can power on the machine; in addition, it needs to short-connect these pins to build the working power supply under battery mode.
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Classification of signal

Classification	Signal Name	Detail Signal
<b>Analog signal</b>	Output load current	RO/P_I-;RO/P_I+
		SO/P_I-;SO/P_I+
		TO/P_I-;TO/P_I+
	INV inductance current	RINV_I-; RINV_I+
		SINV_I-; SINV_I+
		TINV_I-; TINV_I+
	Output load voltage	RO/P.N;RO/P.L
		SO/P.N;SO/P.L
		TO/P.N;TO/P.L
	Output INV voltage	RINV.N;RINV.L
		SINV.N;SINV.L
		TINV.N;TINV.L
	INV VDC	RINVDC-;RINVDC+
		SINVDC-;SINVDC+
		TINVDC-;TINVDC+
	BUS voltage	+BUS.N;+BUS
		-BUS.N;-BUS
	UPS input main power voltage	RLINE.N;RLINE.L
		SLINE.N;SLINE.L
		TLINE.N;TLINE.L
	Bypass voltage	RBPS.N;RBPS.L
		SBPS.N;SBPS.L
		TBPS.N;TBPS.L
	PFC inductance current	RPFC-CT+;RPFC-CT-
		SPFC-CT+;SPFC-CT-
		TPFC-CT+;TPFC-CT-
		RPFC+CT+;RPFC+CT-
SPFC+CT+;SPFC+CT-		
Input battery voltage	+BAT.N;+BAT	
	-BAT.N;-BAT	

	Temperature sampling signal	THRM0; THRM1; THRM2;THRM3
--	-----------------------------	---------------------------

Classification	Signal Name	Detail Signal
<b>Control signal</b>	INV PWM	RINVPWM-; RINVPWM+
		SINVPWM-; SINVPWM+
		TINVPWM-; TINVPWM+
	PFC PWM	RPFCPWM-; RPFCPWM+
		SPFPCWM-; SPFPCWM+
		TPFPCWM-; TPFPCWM+
	Control signal of output RELAY	INVRELAY2; INVRELAY3; INVRELAY4
	SHUNTDONW signal	SD
	Signal of working power supply set	SW
	Power signal	SW_ON
	Sampling signal of physical address	LOC1; LOC2; LOC3; LOC4
	Hot-plugging signal	HOT-SWAP
	Synchronizing signal	OS-SYN-; OS-SYN+
	Synchronizing pulse signal	HOSTSYN-; HOSTSYN+
	CAN communication signal	CANH;CANL
	SCR signal of switching of main power and battery	LINESCR
		BATSCR
	Control signal of rotate speed of the fan	FANSPEED
	Detection signal of condition of the fan	FANDET0; FANDET1; FANDET2
	EPO signal	EPO
	Control signal of BUS soft start	DCSTART
	Communication signal of serial port	IPOMSRXD;IPOMSTXD
	LED signal in front of UPS module	LED
Sampling signal of disconnected line of parallel machine	PAR-DET	
BYPASS signal	STS	

Classification	Signal Name	Detail Signal
Power supply and ground	Primary side power supply	12V、15V、-15V、5V

	Primary side ground	GND
	Secondary side power supply	+VCC、+15V (I)
	Secondary side ground	GNG(ISP)

### 3. Principle of Charger module

#### 3.1 The introduction of charger module

##### 3.1.1 The introduction of charger

The charger module is mainly composed by charger BUCK module as shown at Figure3.1.1. It can reduce the inputted  $\pm$ BUS voltage to targeted voltage value which can be adjusted by voltage of 16-20 pieces of batteries to supply power for two groups of batteries respectively. It can provide the battery groups the equalized voltage of 14.25V/pcs and the float voltage of 13.35V/pcs. Single charger can provide the maximum 12A charging current, which is settable from 1 to 12A. Double charger can provide the maximum 24A charging current, which is settable from 1-24A.

##### 3.1.2 Schematic circuit of CHGR\_PSDR and dial switch for battery

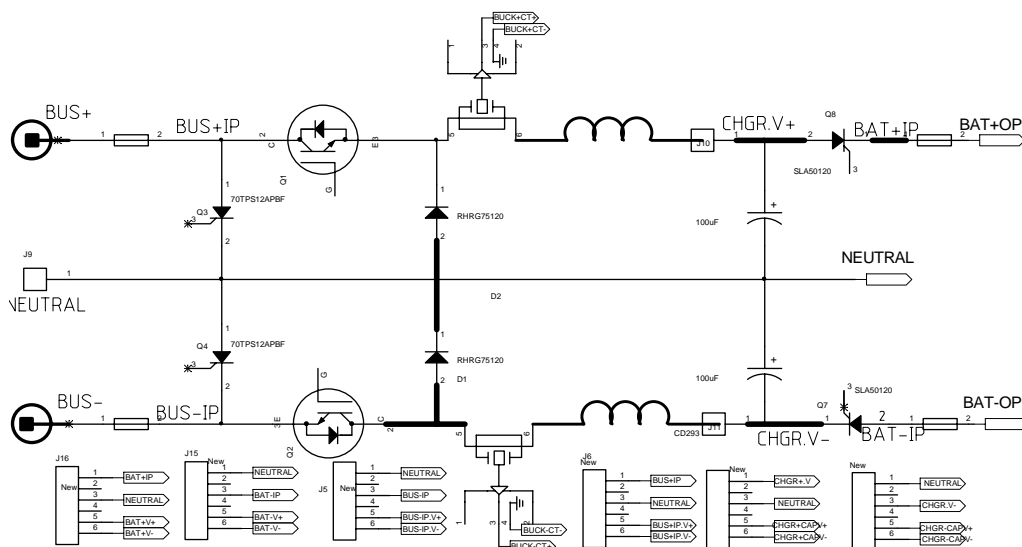


Figure 3.1.1 Schematic Circuit of CHGR\_PSDR

Batteries	Equalized Voltage(V)	Float Voltage(V)
16	228	213.6
17	242.2	227
18	256.5	240.3
19	270.7	253.6
20	285	267

Chart 3.1.1 Charger output for different battery groups

Battery protection	1	2	3	4
20PCS	0	0	0	0
19PCS	1	0	0	0
18PCS	1	1	0	0
17PCS	1	1	1	0
16PCS	1	1	1	1



Chart3.1.2 Dial switch of battery (ON=1,OFF=0)

### 3.2 Auxiliary power supply module (SPS)

#### 3.2.1 The introduction of SPS module

Structure of main circuit of SPS is the structure of FLYBACK transformer. After pressing button of power on after the main power is supplied under main power mode or battery mode, the IC3845 will build a working power supply and start to work, and the driving output pin will output PWM wave form to drive the MOS pipe. When MOS pipe is on, original edge of transformer will store the energy and there is no output for the secondary edge; when MOS pipe is off, energy of transformer will be transferred to all circuits of secondary edge to produce  $\pm 15V$ ,  $+12V$ ,  $+5V$  and FAN12V power supply to supply needed working power supply for the charger module.

#### 3.2.2 Schematic circuit and physical map of SPS

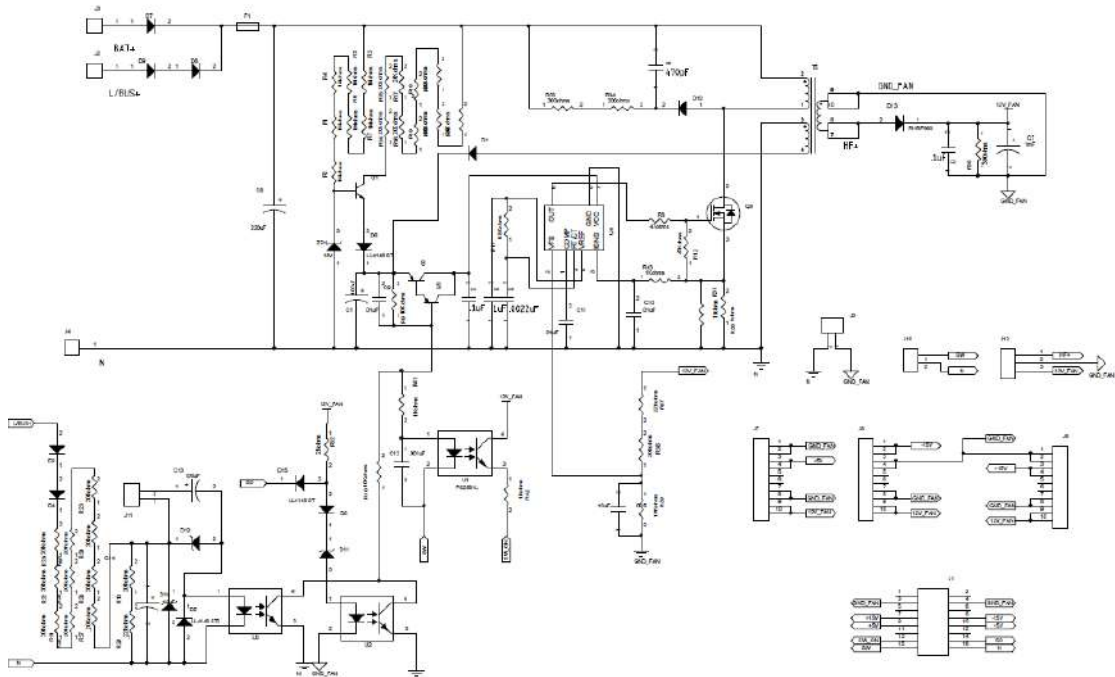


Figure 3.2.1 Schematic Circuit of SPS of Charger Module



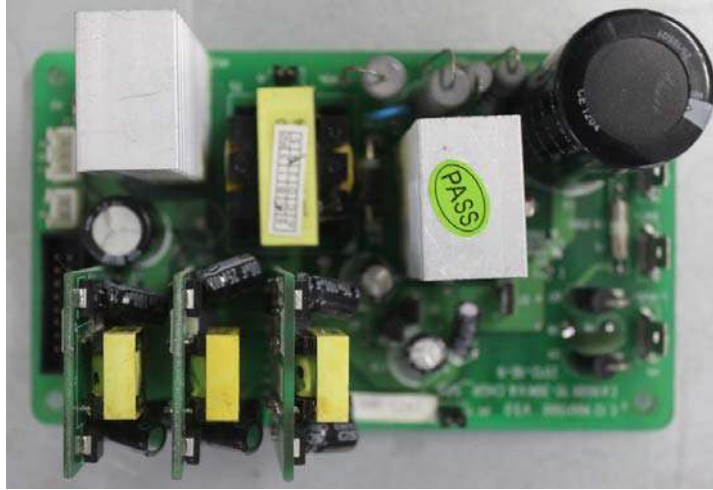


Figure 3.2.2 Physical Map of SPS

### 3.2.3 Explanation for signal interface of SPS of Charger Module

NO.	Interface	Label	Explanation	Notes
J3	J3	BAT+	Supply positive voltage of battery to +BUS	Input
J2	J2	L/+BUS	main power input	
J4	J4	N	N cable of main power input	
J10	1	SW	Control signal of SPS start	Control
	2	N	N line	
J12	1	HF+	HF+ High frequency pulse signal	Output signal
	2	GND_FAN	Output ground used to supply power the fan	
	3	12V_FAN	Output 12V DC used to supply power to the fan	
J1	3/4	GND_FAN	Output ground used to supply power the fan	
	7	+15V	DC +15V	
	8	-15V	DC -15V	
	9/10	+5V	DC +5V	
	13	SW_ON	Power signal (used for single module debugging)	
	14	SD	SPS can be stopped by this signal	

	15	SW	SW signal	
	16	N	N line	

### 3.3 CHGR\_CNTL

#### 3.3.1 Introduction of the function of CHGR\_CNTL

Transfer the analog signal received into control signal output to control the Charger to work according to requirements under different conditions. And communicate with power module and monitor module.

#### 3.3.2 Physical map of CHGR\_CNTL



Figure 3.3.1 Physical map of CHGR\_CNTL

#### 3.3.3 Explanation for signal interface of CHGR\_CNTL

Interface matching

NO.	Interface	Explanation
1	CN802	Matching CHGR_PSDR J49
2	CN008	Matching Power module J6
3	CN2	Matching RS232 CN1
4	CN3	Matching INTERFAC J18 or J19
5	CN5	Matching CHGR_PSDR CN5
6	CN11	Matching CHGR_PSDR CN11
7	CN4	No connect
8	CN801	No connect, start the charger manually by short CN801 for 3s
9	CN800	No connect, connect to +5V power when download program

CN802:

NO.	Interface	Label	Explanation	Notes
CN802	1	+VCC3	+12V	
	2	GND-S3	Ground	

CN008:

NO.	Interface	Label	Explanation	Notes
CN008	1	RESERVEDIO1	Reserved	
	2	RESERVEDIO2	Reserved	
	3	GND_12V	Ground	

	4	+12V	+12V	Power Module
	6	CHGON	Charger on/off signal	Low level effective
	7	NCHGVOLT	Control signal for negative buck	Low level effective
	8	PCHGVOLT	Control signal for positive buck	Low level effective

CN2:

NO.	Interface	Label	Explanation	Notes
CN2	1	RS232_TX	RS232 Send	
	2	RS232_RX	RS232 Receive	
	3	GND-S1	RS232 Ground	

CN3:

NO.	Interface	Label	Explanation	Note
CN3	1	RS485-	485 negative	
	2	RS485+	485 positive	
	3	GND_485	485 GND	
	4	12V_485	485 +12V	
	7	INTERFACE_LOCATION_GND	INTERFACE_LOCATION_GND	Matching INTERFACE J18 or J19
	8	INTERFACE_LOCATION	INTERFACE_LOCATION	
	9	GND-S3	Ground	
	10	+VCC3	+VCC3	

CN5 (sampled signal port) :

NO.	Interface	Label	Explanation	Notes
CN5	3/4	-CHGR.V/ -CHGR.N	Negative BUCK voltage	
	5/6	+CHGR.V/ +CHGR.N	Positive BUCK voltage	
	7/8	-BAT_IP.V/-BAT_IP.N	-BAT voltage sampled(before FUSE )	
	9/10	+BAT_IP.V/+BAT_IP.N	+BAT voltage sampled(before FUSE )	
	11/12	-BAT.V/-BAT.N	-BAT voltage sampled	
	13/14	+BAT.V/+BAT.N	+BAT voltage sampled	
	15/16	-BUS.V/-BUS.N	-BUS voltage	

			sampled	
	17/18	+BUS.V/+BUS.N	+BUS voltage sampled	
	19/20	-BUS_IP.V/-BUS_IP.N	-BUS voltage sampled	
	21/22	+BUS_IP.V/+BUS_IP.N	+BUS voltage sampled	
	23/24	BAT.TMP1+/BAT.TMP1-	Battery temp.	
	25/26	BAT.TMP2+/BAT.TMP2-	Battery temp.	No used
	27/28	BUCK-.CT+/BUCK-.CT-	-BUCK inductance current	
	29/30	BUCK+.CT+/BUCK+.CT-	+BUCK inductance current	

CN11:

NO.	Interface	Label	explanation	NOTES
CN11	1	HFPOWER+	HFPOWER+	
	2	HFPOWER-	HFPOWER-	
	7	-15V	-15V	
	8	+15V	+15V	
	9/10	+5V	+5V	
	11/12/13/14	GND-D	GND-D	
	15	BATNUM4	Signal for detecting battery num.	
	16	BATNUM3	Signal for detecting battery num.	
	17	BATNUM2	Signal for detecting battery num.	
	18	BATNUM1	Signal for detecting battery num.	
	21	THRM1	Charger1 temp.	
	22	THRM0	Charger 0 temp.	
	23	BATREV_FAULT	Battery reverse polarity detect	Low level effective
	24	CHGR_SCR	SCR control signal	Low level effective
	25	BUCK-PWM	Negative BUCK	Switching

			PWM	frequency
	26	BUCK+PWM	Positive BUCK PWM	47KHZ
	27	FAN_CNTL	Fan speed signal	
	28	FAN_DET	Fan detect	
	29	~SD	Off charger power	Low level effective
	30	FAN_ST	The signal for stop the fan	

### 3.4 CHGR\_PSDR

#### 3.4.1 Introduction of the CHGR\_PSDR

The circuit diagram of CHGR\_PSDR as shown in Figure 3.1.1 and detail describe as shown in Chapter 3.1.1.

#### 3.4.2 Physical map of CHGR\_PSDR

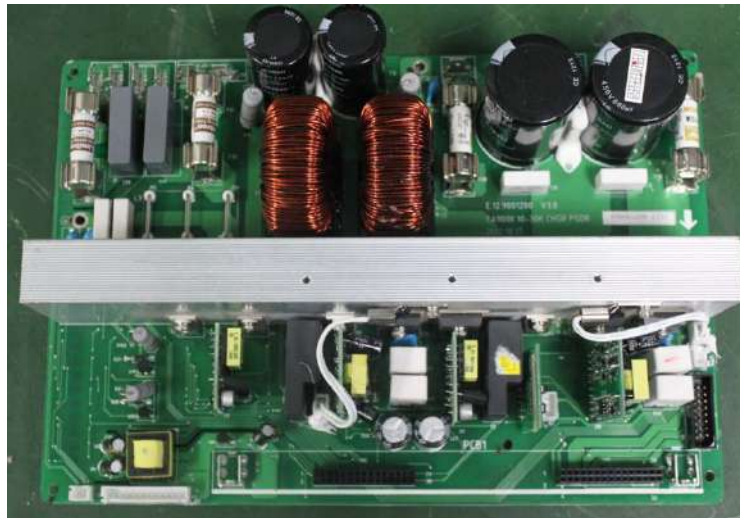


Figure 3.4.1 Physical map of CHGR\_PSDR

#### 3.4.3 Explanation for signal interface of CHGR\_PSDR

NO.	Label	Explanation
J28/J34	+BUS	+BUS input port
J35/J37	NEUTRAL	N port
J29	-BUS	-BUS input port
J30/J32	+BAT	+BAT
J36/J38	NEUTRAL	N
J31/J33	-BAT	-BAT

**Signal:**

**J53 (Fan PORT):**

NO.	Interface	Label	Explanation
-----	-----------	-------	-------------

J53	1	FAN	
	2	12V_FAN	

**J50 (Power Port):**

No.	Interface	Label	Explanation
J50	3/4	GND-D	GND-D
	7	+15V	+15V
	8	-15V	-15V
	9/10	+5V	+5V
	14	SD	shutdown

**J51(Power Port):**

NO.	Interface	Label	Explanation
J51	1	HF+	HF+
	2	GND_FAN	GND
	3	12V_FAN	12V

**J49**

NO.	Interface	Label	Explanation
J49	+VCC3	+VCC3	Matching
	GND-S3	GND-S3	CHGR_CNTL CN802

**J52:**

NO.	Interface	Label	Explanation
J8	1	5V_TMP	+5V
	2	TMP1	
	8	S1	Dial switches for the number of batteries
	9	S2	
	10	S3	
	11	S4	
	12	GND-S3	GND-S3

CN5 and CN11 of CHGR\_PSDR matching the CN5 and CN11 of CHGR\_CNTL respectively.

#### 4. Principle of Monitoring Module

Functional modules of monitoring module include input connecting plate, auxiliary power supply board, communicational power supply board, power socket plate MONITOR OUT\_CON\_Z, MONITOR OUT\_CON\_T, MONITOR IN\_CON\_Z, MONITOR IN\_CON\_T, control panel of monitoring module, LED lamp panel, key-press panel, interface board and LCD panel. The communicational power supply board, input connecting plate, and control panel of monitoring module are introduced as follows.

##### 4.1 Communicational power supply board (COM\_SPS)

###### 4.1.1 Introduction of functions of COM\_SPS

Main circuit structure of COM\_SPS is a structure of FLYBACK transformer. FAN12V supplies the power supply to start the IC3845 so that the output pin can output PWM wave form to



2	J2-5/6	+12V_IN	Input +12V DC
3	J2-14	SD2	Power off signal of SPS
4	J2-15/16	SW2; SW1	Short-connection of these pins under battery mode can build the working power supply

### J3

No.	Interface	Label	Explanation
1	J3-1/3	GND_1	+12V power supply, -12V corresponding ground
2	J3-2/4	+12V;-12V	Output power supply +12V and -12V
3	J3-7	GND_3	+5V_2 corresponding ground
4	J3-8	+5V_2	Output power supply +5V of one group
5	J3-11	GND	+5V_1 corresponding ground
6	J3-12	+5V_1	Output power supply +5V of another group
7	J3-13	SD	Power off signal of SPS
8	J3-14	3.3V	Input 3.3V power supply

## 4.2 Input connecting plate (INPUT\_CNT)

### 4.2.1 Introduction of functions of input connecting plate

Input connecting plate connects the input main power and battery with input terminal of SPS.

### 4.2.2 Schematic circuit and physical map of input connecting plate

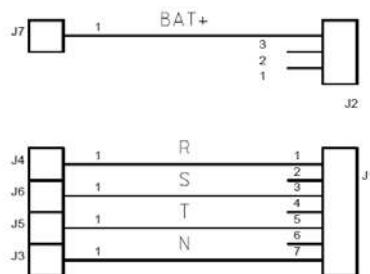


Figure 4.2.1 Schematic Circuit of COM\_SPS



Figure 4.2.2 Physical Map of COM\_SPS

### 4.2.3 Explanation for signal interface of input connecting plate

No.	Interface	Label	Explanation
1	J4	R	Input phase R of three-phase main power
2	J6	S	Input phase S of three-phase main power



3	J5	T	Input phase T of three-phase main power
4	J3	N	Input ground of three-phase main power
5	J7	BAT+	Input battery positive

No.	Interface	Explanation
1	J2	J13 connected to SPS, providing SPS battery positive input
2	J1	J12 connected to SPS, providing SPS main power input

### 4.3 Control panel of monitoring module (MONITOR BOARD)

#### 4.3.1 Introduction of functions of MONITOR BOARD

MONITOR BOARD adopts the chip LM3S2950 for main control to achieve communication between monitoring module and power module, charger module and external module and display the data of working conditions of all machines by LCD screen.

#### 4.3.2 Physical map of MONITOR BOARD



Figure 4.3.1 Physical Map of MONITOR BOARD

#### 4.3.3 Explanation for signal interface of MONITOR BOARD

J5: button/emergent power off interface

J8: interface of LED lamp

J17: Communication port (data from SNMP card, dry node card, USB card, and RS485 card)

J18: CAN communication port

J19: interface of LCD back light

J23: input interface of FAN12V power supply

CN6: power supply input interface of COM\_SPS

CN8: SW1; SW2 (connect with COM\_SPS-J1)

CN9: interface of LCD

## Chapter II Start Debugging of Module

Note: only the debugging steps of modules after maintenance are listed, and other debugging shall refer to rules for debugging of single module.

### 1. Start Debugging of Power Module

#### 1.1 Power on of DC source and BUS voltage sampling

##### Measurement procedures:

- (1) Adjust the output voltage of two DC sources to 240V/1.5A, connect the output terminals of DC sources with positive and negative input terminals of battery of UPS, and then connect two universal meters with positive and negative BUS.
- (2) Take off the IGBT driving board in inverter three-phase, connect the J101, J201, and J301 in IGBT connecting plate with IGBT driving plate specially used for debugging (that is, adding a 2.2K resistance to 8 and 9 (fault) signal pins of this socket).
- (3) Take a normally open not-locking switch as a button of power on to connect with CN011 of control panel, turn on the DC source output, touch the button of power on lightly, and then the UPS will build the working power supply. Press the button of power on for 5s, the relay of soft start board will be closed. BUS voltage is rising from 0, observe the voltage value after the BUS voltage of universal meter is stable until the BUS voltage is up to 360V±2V.
- (4) At the same time, close outputs of two DC sources and discharge the electricity of positive and negative BUS with discharge resistance.

**Note:** for maintained and debugged module, it is suggested to start the PFC of three phases one by one to avoid damaging more boards when starting the machine. It can disconnect phase S and T (can remove SCR driving signal cables of corresponding rectification board) and only connect the phase R to start the machine, and then measure the BUS voltage; connect the phase S and T in order to start the machine, and then measure the BUS voltage.

##### Judgment criteria:

BUS voltage is: 360V±2V.

#### 1.2 Rectification of output voltage and measurement of output frequency

##### Measurement procedures:

- (1) Take down the IGBT driving board specially used for debugging, put original IGBT driving board to original position, and it shall not be misplaced or inverted.
- (2) Turn on the two DC sources, press button of power on for 5s, and the

inverter relay will be closed and light in front panel of the module will be on after about 10s. There is some output for the module then.

- (3) Measure the output voltages of three phases with universal meter separately, debug the software through serial port, and adjust the output voltage to  $221\text{VAC}\pm 0.1\text{V}$ .
- (4) Use oscilloscope or universal meter to measure the frequencies of output voltages in three phases which shall be  $50\text{Hz}\pm 0.5\text{Hz}$ .

**Note:** for maintained and debugged module, it is suggested to start the inverters of three phases one by one to avoid damaging more boards when starting the machine. It can disconnect inverter driving boards in phase S and T which shall be replaced by special tools of measurement and only connect the driving board in phase R to start the machine, and then observe the soft start process of inverter voltage with oscilloscope. Connect the inverter driving boards in phase S and T in order, and then observe the inverter closing process by referring to measurement procedures of inverter in phase R.

**Judgment criteria:**

Output voltage of three phases is:  $221\text{VAC}\pm 0.1\text{V}$ , and output frequency of three phases is  $50\text{Hz}\pm 0.5\text{Hz}$ .

## 2. Start Debugging of Charger module

### 2.1 Main power current-limiting start and BUS voltage sampling

**Measurement procedures:**

- (1) Adjust the output voltage of adjustable AC sources in three phases to  $220\text{V}/2\text{A}$ , connect the outputs of AC source with main power input terminal of charger module, and then connect two universal meters with positive and negative BUS separately.
- (2) Remove the output fuse in CHGR\_PSDR.
- (3) Connect the switch wire used to start the machine with CN801 in control panel, turn on the output of AC source, and then UPS will build the working power supply. Press button of power on for 5s, and then the relay of soft start board will be closed. BUS voltage is rising from 0, observe the voltage value after the BUS voltage of universal meter is stable until the BUS voltage is up to  $360\text{V}\pm 2\text{V}$ .
- (4) Close output of AC source and discharge the electricity of positive and negative BUS with discharge resistance.

**Note:** for maintained and debugged module, it is suggested to start the PFC of three phases one by one to avoid damaging more boards when starting the machine. It can disconnect phase S and T (can remove SCR driving signal cables of corresponding rectification board) and only connect the

phase R to start the machine, and then measure the BUS voltage; connect the phase S and T in order to start the machine, and then measure the BUS voltage.

**Judgment criteria:**

BUS voltage is:  $360V \pm 2V$ .

## 2.2 Measurement of charging voltage

**Measurement procedures:**

- (1) Put the removed output fuse to original places.
- (2) Turn on the AC source, press button of power on for 5s, indicator light in front panel of the module will be on after about 10s. There is some output for the charger module then.
- (3) Within 30s upon the charger is started, measure the positive/negative charging voltage with universal meter which shall be even charging voltage  $285VDC \pm 4V$  (when measuring the single charger module, LCD is not online, the software defaults to set the voltage output as that of 20 pieces batteries, even charging voltage =  $14.25 * \text{pieces of battery}$ , float charging voltage =  $13.35 * \text{pieces of battery}$ , and the voltage accuracy is 2%; what measured within 30s upon starting is even charging voltage.).

**Note:** for maintained and debugged module, it is suggested to start the PFC of three phases one by one to avoid damaging more boards when starting the machine. It can disconnect phase S and T and only connect the phase R to start the machine, and then measure the charging voltage; connect the phase S and T in order to start the machine, and then measure the charging voltage.

**Judgment criteria:**

Positive/negative charging voltage is: even charging voltage is  $285VDC \pm 4V$ .

## Chapter III Fault and Warning Code of Module

### 1. Fault and Warning Code of Power Module

#### 1.1 Warning code of power module

Transformation principle of warning code:

The warning code read through serial port is a combined decimal number, and it needs analysis to get the real warning code.

The transportation process is:

Firstly transform the read decimal number into hexadecimal number which equals the summary of all warning codes. Every warning code only accounts for one bit, so it is easy to know the hexadecimal number is the summary of which warning codes by looking up the warning code table.

For example: if 1684 is read in serial port, and it is 0x0694 by transforming into hexadecimal number, and then  $0x0694 = 0x0004 + 0x0010 + 0x0080 + 0x0200 + 0x0400$ . In this way, it is known that 1684 is 5 warnings.

Num	Low warning code	Interpretation
1.	0x0001	EPO
2.	0x0002	Fault of output overload (exceeding the overload time)
3.	0x0004	CAN communication is abnormal.
4.	0x0008	Overload of output
5.	0x0010	Battery is disconnected.
6.	0x0020	ECO unsteady
7.	0x0040	Over-current of output
8.	0x0080	Difference between main power and bypass
9.	0x0100	Battery voltage abnormal
10.	0x0200	Read-write of EEPROM is in error.
11.	0x0400	Fault of fan
12.	0x0800	Phase sequence of main power is in error.
13.	0x1000	Phase sequence of bypass is in error.
14.	0x2000	Loss of N cable
15.	0x4000	Fault of synchronizing signal
16.	0x8000	Fault of synchronizing pulse
17.	High warning code	
18.	0x0001	Main power is abnormal.
19.	0x0002	Bypass is abnormal.
20.	0x0004	Low voltage of battery
21.	0x0008	Retaining
22.	0x0010	Charger is not online.
23.	0x0020	Retaining
24.	0x0040	Frequency of bypass is abnormal.
25.	0x0080	Overvoltage of output
26.	0x0100	Physical address is abnormal.
27.	0x0200	PFC in phase R is abnormal.
28.	0x0400	PFC in phase S is abnormal.
29.	0x0800	PFC in phase T is abnormal.
30.	0x1000	Relay abnormal
31.	0x2000	Bypass STS disconnect

32.	0x4000	Bypass STS short
33.	0x8000	Quit ECO abnormal

## 1.2 Fault code of power module

Num	Fault code	Whether it has bypass output after the fault or not	Interpretation
1.	1	YES	High voltage of BUS
2.	2	YES	Low voltage of BUS
3.	3	YES	Unbalance of BUS
4.	4	YES	Short-circuit of BUS
5.	5	YES	Bypass wiring error
6.	6	YES	Soft start of BUS is overtime.
7.	7	YES	Soft start of inverter is overtime.
8.	8	YES	High voltage of inverter
9.	9	YES	Low voltage of inverter
10.	10	NO	Output short-circuit in R phase
11.	11	NO	Output short-circuit in S phase
12.	12	NO	Output short-circuit in T phase
13.	13	NO	Output short-circuit in RS phase
14.	14	NO	Output short-circuit in ST phase
15.	15	NO	Output short-circuit in TR phase
16.	16	YES	Output negative work in phase R is abnormal.
17.	17	YES	Output negative work in phase S is abnormal.
18.	18	YES	Output negative work in phase T is abnormal.
19.	19	NO	Overload fault
20.	20	NO	Battery of the module is abnormal.
21.	21	YES	Retaining
22.	22	YES	Over-temperature fault

23.	23	YES	Fault of synchronizing signal
24.	24	YES	Fault of synchronizing pulse
25.	25	YES	Sticking of relay
26.	26	YES	Fault of main power SCR
27.	27	YES	Fault of CAN bus
28.	28	YES	Fault of total negative work
29.	29	YES	Physical address is conflict.
30.	30	NO	IGBT is in short-circuit (useless)
31.	31	NO	Inverter abnormal
32.	32	NO	Power setting error

## 2. Fault and Warning Code of Charger module

### 2.1 Warning code of charger module

Num	Warning code	Interpretation
1.	0x0001	Battery is over charged.
2.	0x0002	Battery is connected inversely.
3.	0x0004	Battery is disconnected.
4.	0x0008	Charger is abnormal.
5.	0x0010	Charger is in short circuit.
6.	0x0020	None
7.	0x0040	Charger suicide
8.	0x0080	Communication of charger is abnormal.
9.	0x0100	Physical address is in error.
10.	0x0200	LCD is not online.
11.	0x0400	Set of charging voltage is in error.
12.	0x0800	Set of charging current is in error.
13.	0x1000	EPO enable
14.	0x2000	Fault of fan
15.	0x4000	Phase sequence of main power is in error.
16.	0x8000	Loss of N cable

### 2.2 Fault code of charger module

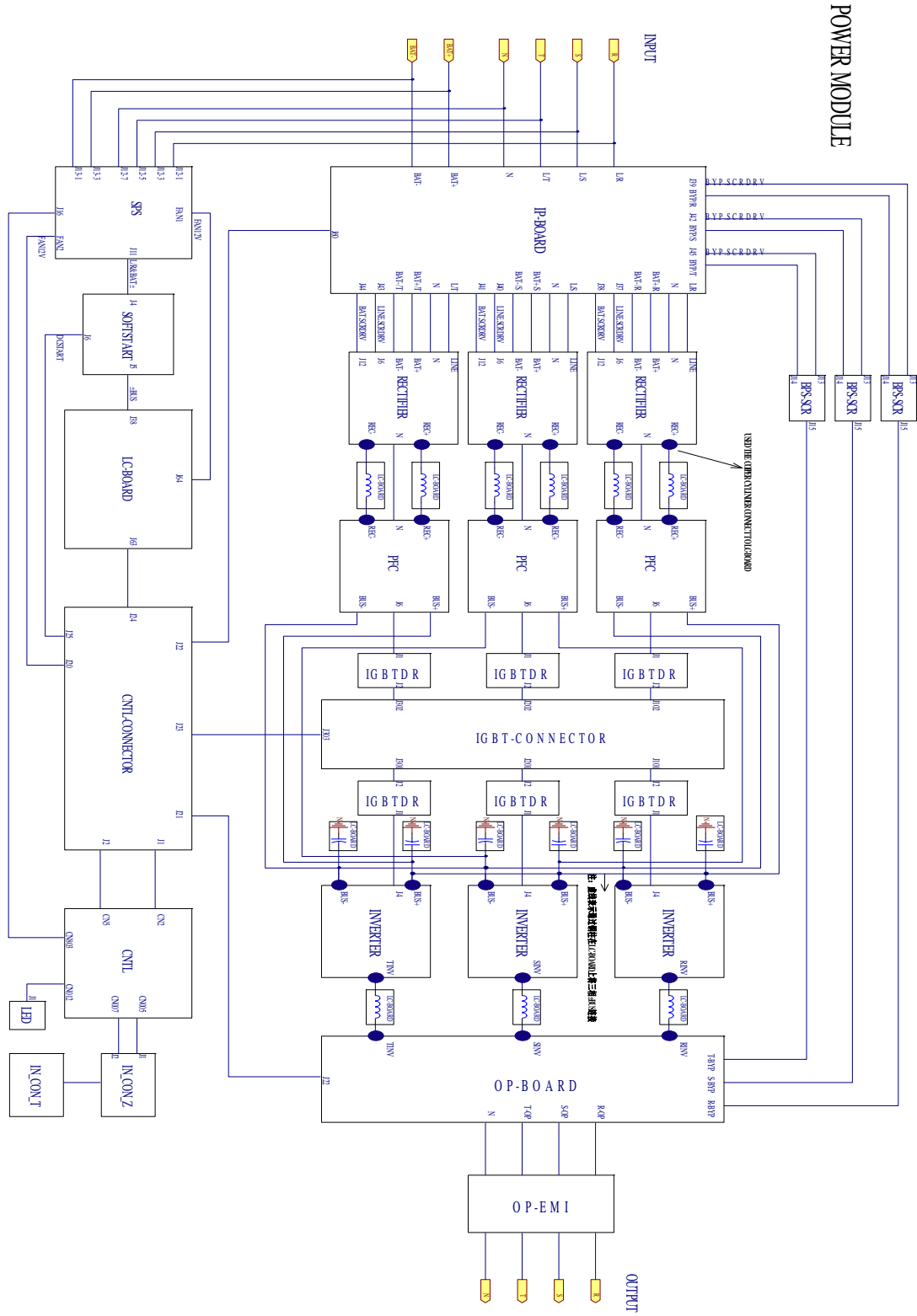
Num.	Fault code	Interpretation
1.	1	BUS soft start fail
2.	2	BUS soft start fail
3.	3	

4.	4	
5.	5	Short-circuit in charger
6.	6	Short-circuit in charger
7.	7	Battery polarity reverse
8.	8	Relay of charger is abnormal
9.	9	Input fuse disconnect
10.	10	Input fuse disconnect
11.	11	Output fuse disconnect
12.	12	Physical address of charger is in error.
13.	13	Physical address of charger is in error.



# Appendix:

## 1. Connection Diagram of Single Board of Power Module



## 2. Connection Diagram of Single Board of Monitoring Module

